EXHIBIT 24

Appendix A1

Analysis of Infringement of U.S. Patent No. 6,660,651 by Western Digital Corporation
(Based on Public Information Only)

Plaintiff Ocean Semiconductor LLC ("Ocean Semiconductor"), provides this preliminary and exemplary infringement analysis with respect to infringement of U.S. Patent No. 6,660,651, entitled "ADJUSTABLE WAFER STAGE, AND A METHOD AND SYSTEM FOR PERFORMING PROCESS OPERATIONS USING SAME" (the "'651 patent") by Western Digital Corporation ("WD"). The following chart illustrates an exemplary analysis regarding infringement by Defendant WD's semiconductor products, systems, devices, components, integrated circuits, and products containing such circuits, fabricated or manufactured using ASML's semiconductor fabrication or manufacturing equipment and/or platforms (e.g., ASML's TWINSCAN system). Such products include, without limitation, automotive products (e.g., iNAND® AT EU312, iNAND® AT EM122, iNAND® AT EM132, Automotive AT LD332, AT 132 (e.g., grades 2 and 3), AT 122 (e.g., grades 2 and 3), Industrial Wide Temp IX QD332, Industrial Ext Temp IX QD332, Industrial Ext Temp IX QD334, Industrial Wide Temp IX QD342, Commercial CL SN720, Commercial CL SN520), connected home products (e.g., iNAND® CH EM123/133, CH LD313, CH LD513, CH QD313, CH QD513, CH XB 513, CH XB 313, WD AV-25, WD AV-GP 1000, CL SN720, CL SN520, PC SA530), industrial and IoT products (e.g., iNAND® IX EM132, iNAND® IX EM122, iNAND® IX EU312, iNAND® IX MC EM131, Industrial IX LD342, Industrial IX LD332, Industrial IX QD342, Industrial IX QD332, Industrial IX QD334, Commercial CL SN720, Commercial CL SN520, Commercial PC SN730, Commercial X600, Commercial PC SA530), mobile products (e.g., MC EU521, MC EU511, MC EU311/d, MC EM131/c, MC EM121/b, MC EM111/a, Commercial CL QD501, Commercial CL QD301, Commercial CL QD101), and surveillance products (e.g. CL EM132/122, IX EM122 Wide Temp, IX EM122 Extended Temp, WD PurpleTM SC QD101 Ultra Endurance microSDTM Card), flash memory (e.g., 3D flash and NAND flash), RISC-V SweRVCore Family (e.g., EH1 and EH2) , and similar systems, products, devices, and integrated circuits ("'651 Infringing Instrumentalities").

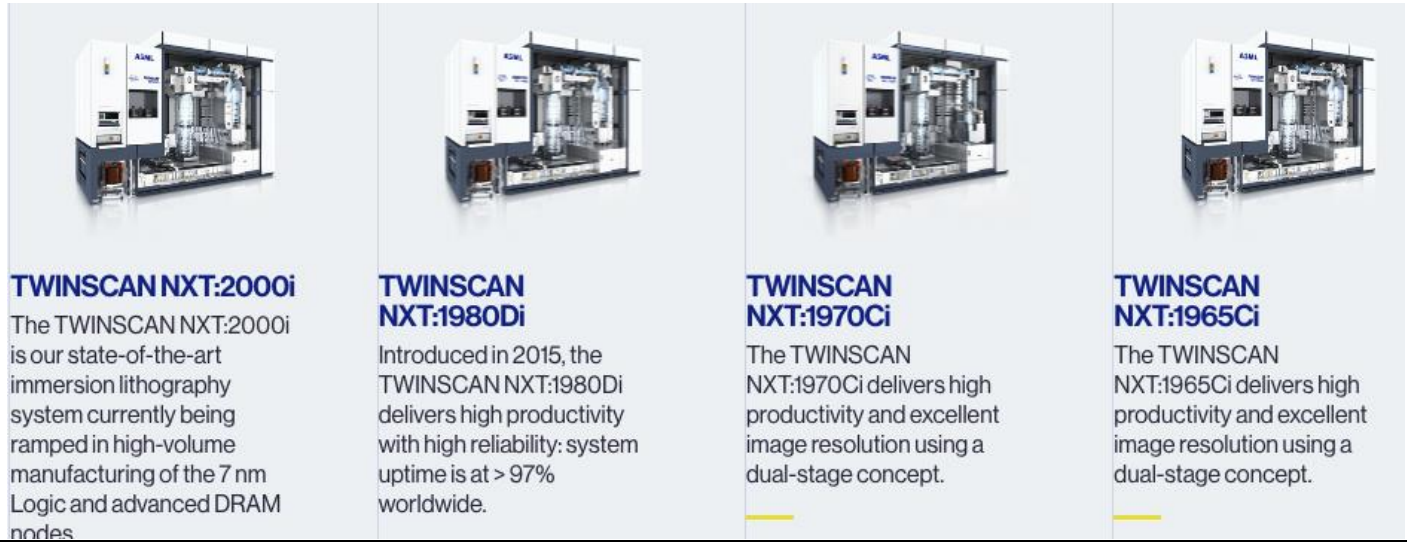
The analysis set forth below is based only upon information from publicly available resources regarding the '651 Infringing Instrumentalities, as WD has not yet provided any non-public information.

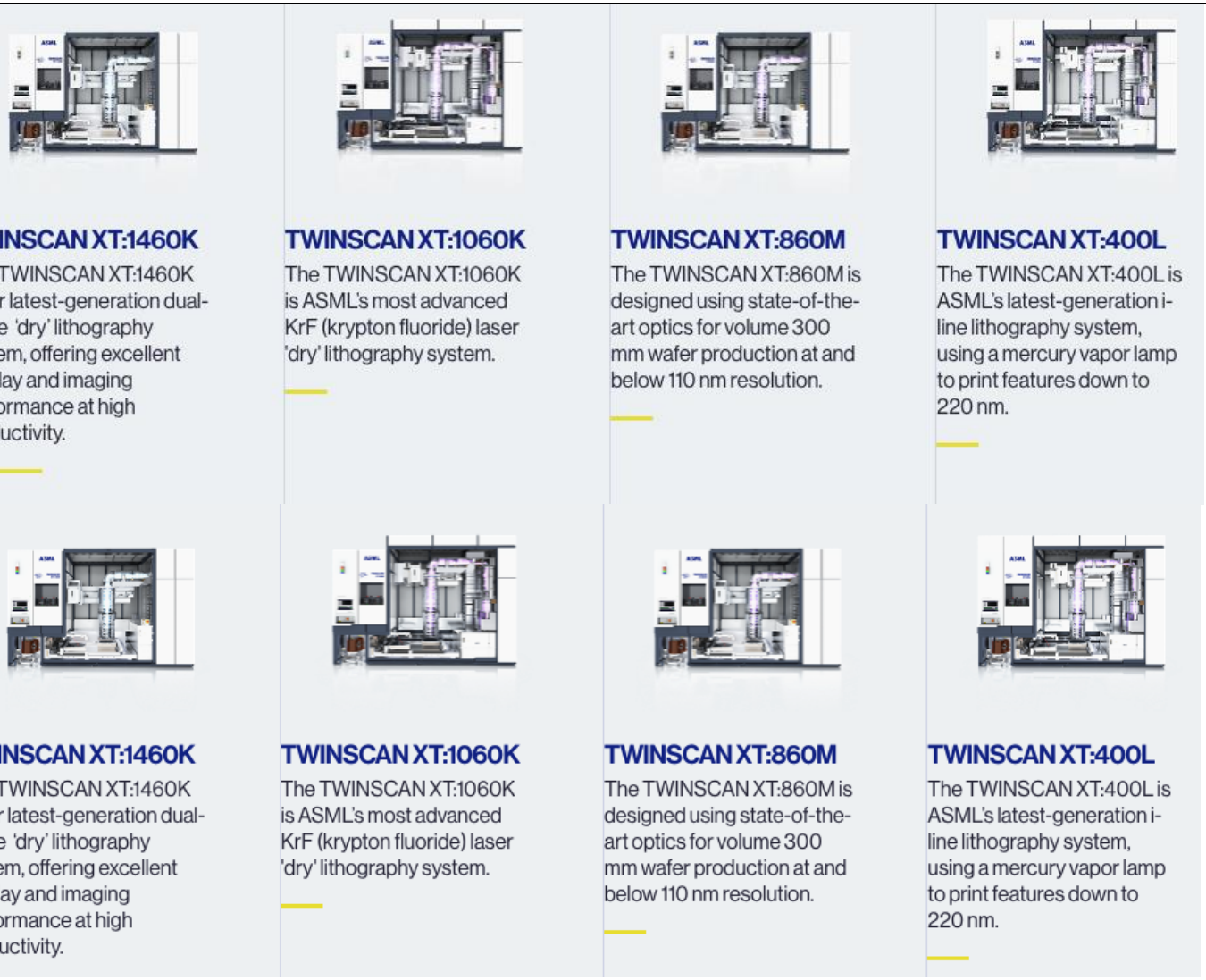
Unless otherwise noted, Ocean Semiconductor contends that WD directly infringes the '651 patent in violation of 35 U.S.C. § 271(g) by using, selling, and/or offering to sell in the United States, and/or importing into the United States, the '651 Infringing Instrumentalities. The following exemplary analysis demonstrates that infringement. Unless otherwise noted, Ocean Semiconductor further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. § 271(b) in conjunction with other evidence of liability.

Unless otherwise noted, Ocean Semiconductor believes and contends that each element of each claim asserted herein is literally met through WD's provision or importation of the '651 Infringing Instrumentalities. However, to the extent that WD attempts to allege that any asserted claim element is not literally met, Ocean Semiconductor believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the '651 Infringing Instrumentalities, Ocean Semiconductor did not identify any substantial differences between the elements of the patent claims and the corresponding features of the '651 Infringing Instrumentalities, as set forth herein. In

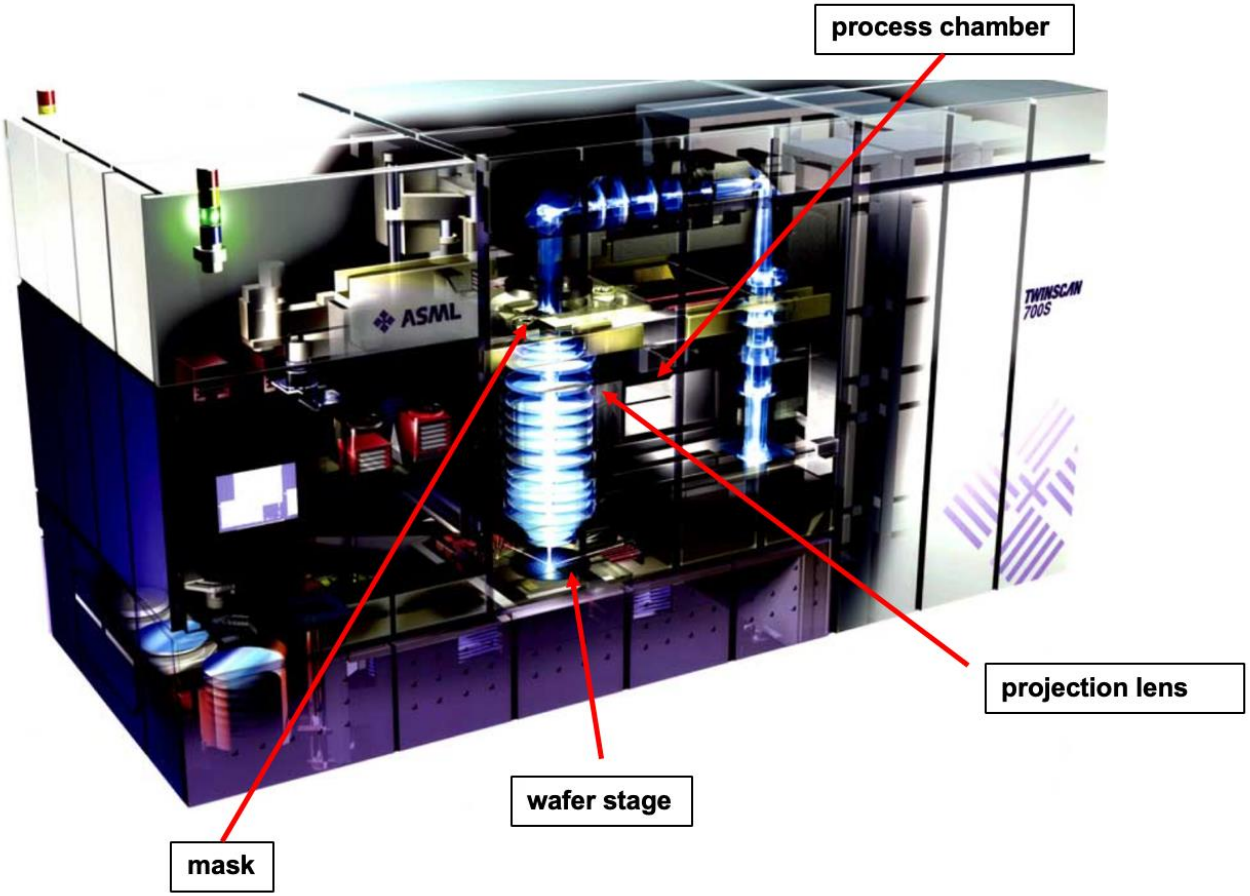
each instance, the identified feature of the '651 Infringing Instrumentalities performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

Ocean Semiconductor notes that the present claim chart and analysis are necessarily preliminary in that Ocean Semiconductor has not obtained substantial discovery from WD nor has WD disclosed any detailed analysis for its non-infringement position, if any. Further, Ocean Semiconductor does not have the benefit of claim construction or expert discovery. Ocean Semiconductor reserves the right to supplement and/or amend the positions taken in this preliminary and exemplary infringement analysis, including with respect to literal infringement and infringement under the doctrine of equivalents, if and when warranted by further information obtained by Ocean Semiconductor, including but not limited to information adduced through information exchanges between the parties, fact discovery, claim construction, expert discovery, and/or further analysis.

USP No. 6,660,651	Infringement by the ’651 Infringing Instrumentalities
19. A method, comprising: providing a process chamber comprised of a wafer stage, said wafer stage having a surface that is adjustable;	The ’651 Infringing Instrumentalities provide a process chamber comprised of a wafer stage, the wafer stage having a surface that is adjustable. For example, each TWINSCAN system includes a process chamber. *See* ASML Corporate Responsibility Report 2015, *available at* https://www.sec.gov/Archives/edgar/data/937966/000093796616000015/corporateresponsibiltyrepo.htm; *see also* ASML products, *available at* https://www.asml.com/en/products/duv-lithography-systems: 

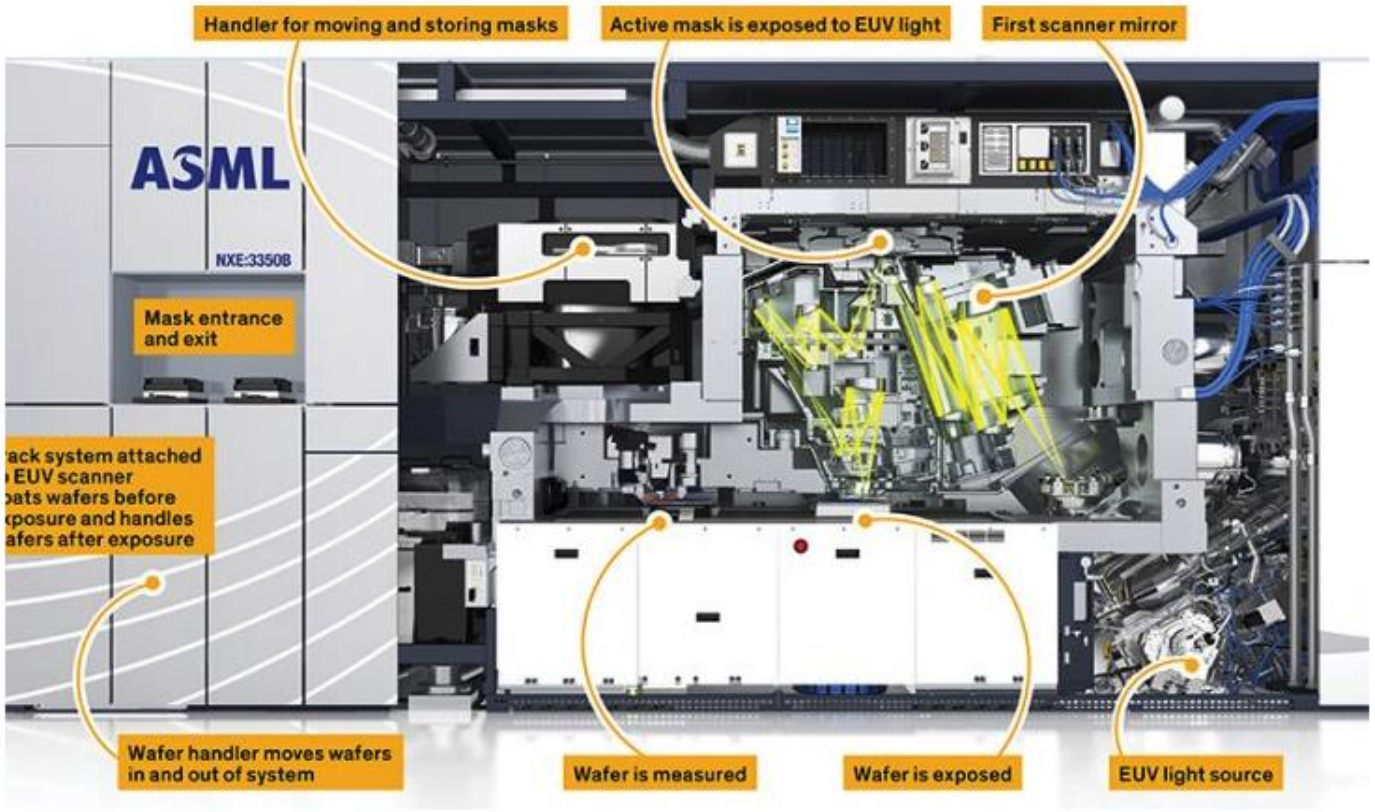


As an example, each TWINSCAN system includes a process chamber as shown below:



See ASML Twinscan Technical Backgrounder, *available at* https://www.chiphistory.org/landmarks/lm_asml_twinscan_step_and_scan_aligner_1990/ip_asml_twinscan_step_and_scan_aligner_1990.htm (annotated).

See also EUV Lithography tools shipping in 2018, available at https://www.nextbigfuture.com/2017/04/euv-lithography-tools-shipping-in-2018.html:



TSMC uses, for example, ASML's extreme ultraviolet (EUV) lithography systems on 5nm and 7nm products. *See e.g.*, TSMC 5nm Technology, *available at* https://www.tsmc.com/english/dedicatedFoundry/technology/5nm.htm ("TSMC's 5nm Fin Field-Effect Transistor (FinFET) process technology is optimized for both mobile and high performance computing applications. It is scheduled to start risk production in the second half of 2019. TSMC's 5nm technology is the second available EUV process technology. It showed promising imaging capability with expected good wafer yield."); *see also TSMC Celebrates 25th Anniversary of the North American Technology Symposium, available at* https://www.tsmc.com/tsmcdotcom/PRListingNewsAction.do?action=detail&language=E&newsid=THGOWQTHTH ("The World's first commercially available 7nm EUV in volume production in 2019").

As another example, the TWINSCAN system performs the method of providing a process chamber:

See ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30 2019).

The process chamber can be used for wafer exposure during lithography:

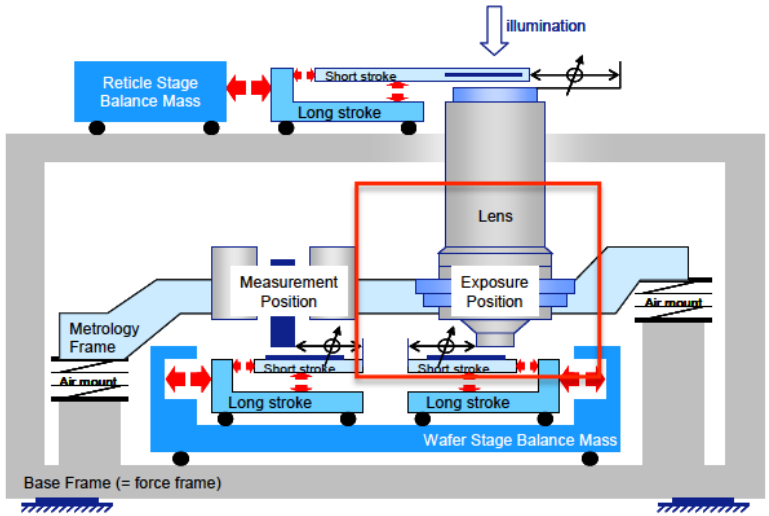


Figure 5. TWINSCAN™ dynamic architecture

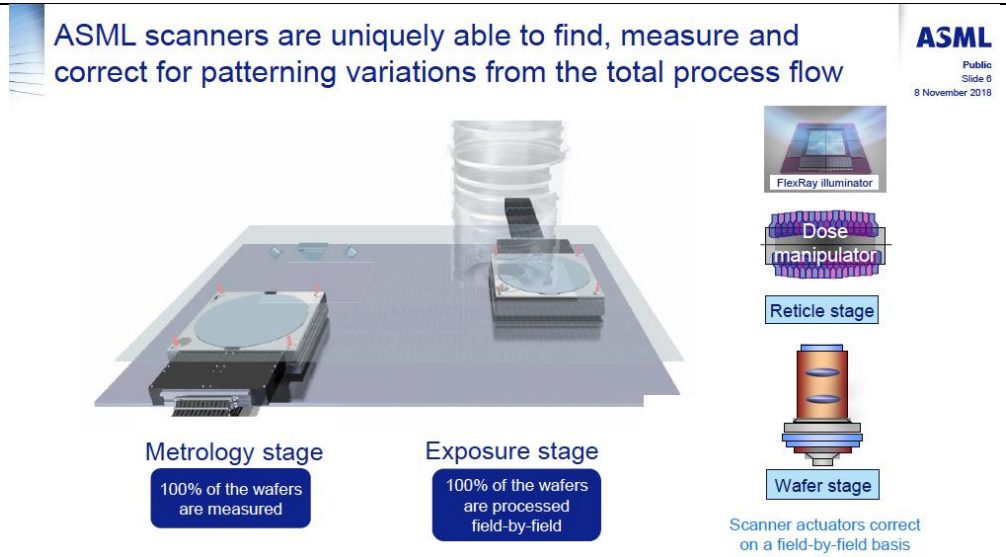
See See H. Butler, ASML Fellow, "A perspective on stage dynamics and control," Mechatronic Systems Development, at 3, *available at* https://pdfs.semanticscholar.org/e49e/90dc78072b03036012e69a913fdfe4ddb935.pdf (last visited Apr. 30, 2020) ("Perspective on Stage Dynamics and Control") (annotated).

The process chamber includes an adjustable wafer stage having a surface that is adjustable:

"In Figure 4, the table holding the wafer is called the mirror block because of the mirroring side surfaces, which allow interferometric position measurement (IFM)."

See H. Butler, ASML Fellow, "Position Control in Lithographic Equipment [Applications of Control]," IEEE Control Systems (Nov. 2011), at 31 *available at* https://www.researchgate.net/profile/Hans_Butler/publication/224258614_Position_Control_in_Lithographic_Equipment_Applications_of_Control/links/5570590b08ae193af41ff41e/Position-Control-in-Lithographic-Equipment-Applications-of-Control.pdf (last visited Apr. 30, 2020) ("Position Control").

For example, the adjustable wafer stage or mirror block of the TWINSCAN system is shown below:

	 *See* Applications Products and Business Opportunity at 6.
adjusting said surface of said wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage to accomplish at least one of raising, lowering and varying a tilt of said surface of said wafer stage;	The ’651 Infringing Instrumentalities adjust the surface of the wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage to accomplish at least one of raising, lowering and varying a tilt of said surface of said wafer stage. For example, the TWINSCAN system adjusts the surface of the wafer stage by raising, lower, or tilting via wafer leveling using vertical actuators (e.g., in the “z direction”): “Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively.” *See* Position Control at 41; *see also id.* at 38 (“For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metro-frame world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor.”). As another example, the TWINSCAN system actuates one of the six Lorentz actuators that are mounted between the air foot and the wafer stage to accomplish at least one of raising, lowering and varying a tilt of the surface of the wafer stage:

	"Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively." *See* Position Control at 41. Generally, the wafer stage is equipped with DOF Lorentz actuators (e.g., three DOF actuators for the horizontal directions and three DOF actuators for the vertical directions): "The table also had vertical movement directions for the purpose of focusing the wafer in the image plane of the lens, requiring a measurement of the distance of the wafer to the lens by means of a level sensor system. The horizontal stage position was measured by an interferometer system. The stage was guided by means of mechanical bearings 'rolling' over the motor beams. With regard to controlling the stage, the horizontal controllers (3-DOF) acted independently from the vertical directions (also 3-DOF)." *See* Perspective on Stage Dynamics and Control at 1. As an example, for the x and y direction, the wafer table is adjusted by three Lorentz actuators such that the stage floats over a granite stone by means of an air bearing and the Lorentz actuators are connected to this granite stone:

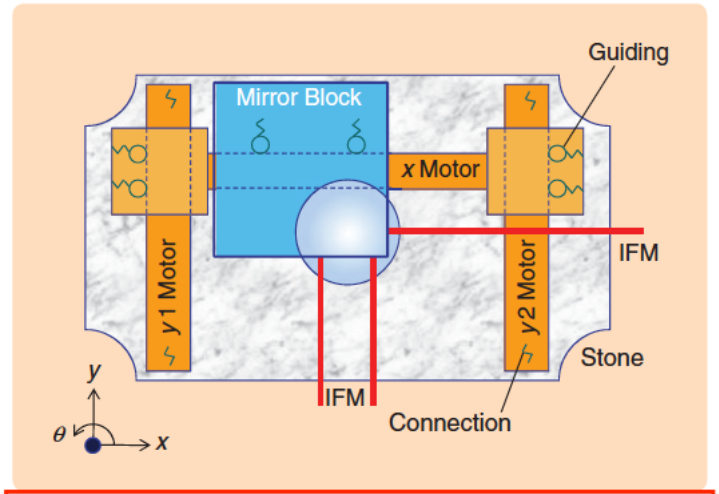


FIGURE 5 Wafer stage top view. The wafer table is driven by three actuators, two of which drive the stage in the *y* direction and the remaining one in the *x* direction. The linear actuators also function as a guide for the horizontal motion, cooperating with ball bearings in the mover. The stage floats over a granite stone by means of an air bearing, and the linear actuators are connected to this stone as well. Interferometers measure the stage position, making use of mirroring side surfaces of the stage.

See Position Control at 31 (annotated).

In total, the TWINSCAN includes 6-DOF Lorentz actuators and 6-DOF stage control, in addition to offline leveling:

"In TWINSCAN™, a further perfection in the basic design was made by using balance masses, full 6-DOF Lorentz actuators and 6-DOF stage control, in addition to off-line levelling."

See Perspective on Stage Dynamics and Control at 3.

As another example, the vertical directions of the wafer stage can be achieved using Lorentz actuators:

"To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result"

See Position Control at 40.

A diagram showing the vertical connection that facilitates the vertical movement of the wafer stage is shown below:

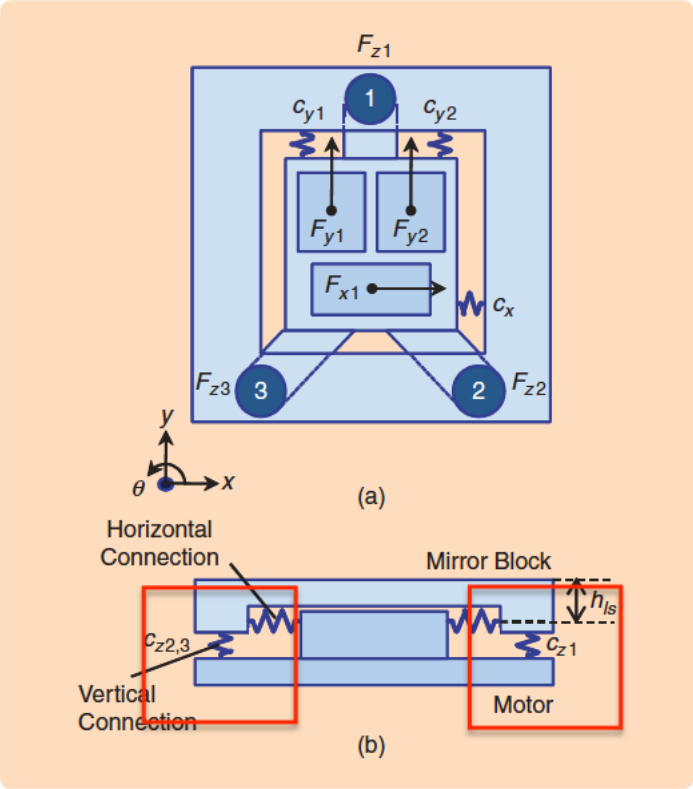


FIGURE 26 Stage layout with motor connection stiffness. The motor

See Position Control at 41 (annotated).

In one example, the wafer stage rotates around the center of the lens above it in the vertical directions using the actuators:

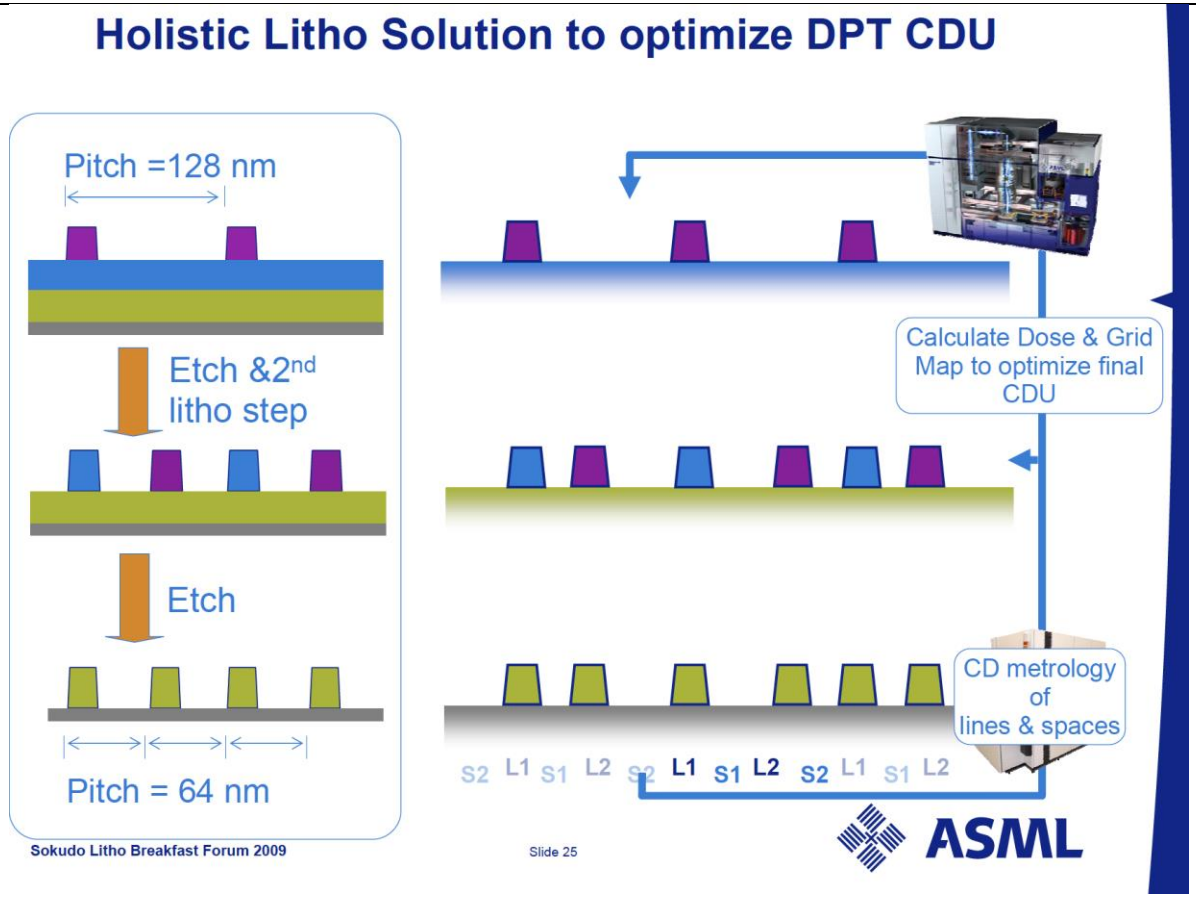
"The stage now rotates around the lens center instead of its center of mass. Especially in the vertical directions, the applicable rotations may show a high acceleration, depending on the vertical topology of the wafer surface."

See Position Control at 42.

	The wafer stage can also be tilted to help keep the wafer in focus: "The reason for this lies in the scanning levelling: when the stage has to tilt around a horizontal axis to keep the wafer in focus, the stage tends to rotate around its center of mass, introducing a horizontal shift on wafer level." *See* Perspective on Stage Dynamics and Control at 2.
positioning a wafer on said wafer stage; and	The '651 Infringing Instrumentalities position a wafer on the wafer stage. For example, the TWINSCAN system positions the wafer on the wafer stage: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35. The wafer is also positioned onto the wafer stage so that exposure can start: "At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40.
performing a process operation on said wafer positioned on said wafer stage.	The '651 Infringing Instrumentalities perform a process operation on the wafer position on the wafer stage. For example, the TWINSCAN system performs stepper imaging or double patterning as part of the step-and-scan in exposing a wafer: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35.

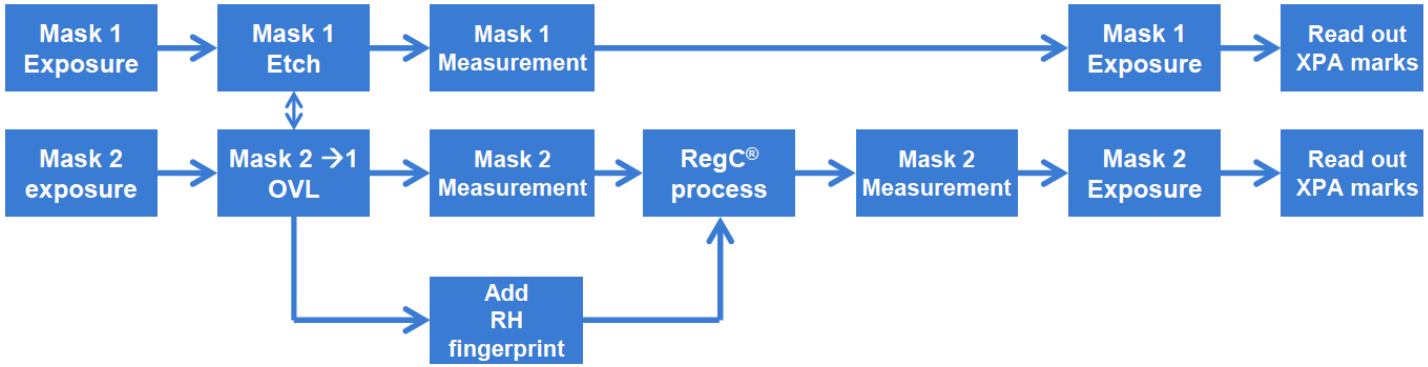
	Once the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself, the stage positioned under the projection lens is aligned to the reticle by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start: "Stage position measurement is now performed in all degrees of freedom by interferometers, with reference beams directed at the projection lens. This method provides a direct relative measurement of the position with respect to the lens. At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40. As another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage, as shown below: "A solution was found by equipping the system with two wafer stages [7]. While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. The increased stage acceleration and speed further improves throughput." *See* Position Control at 39-40; *see also id*. at 37: "Figure 16 shows a more detailed timing diagram of the stage movement during a scan. Figure 16(b) shows an acceleration setpoint profile, which in this example is a thirdorder profile instead of the previously used second-order profile. Figure 16(a) shows the velocity setpoint profile. At t5t0, the acceleration phase ends, and a constant velocity is reached. After a certain settling time, which allows the remaining controller error to be reduced to an acceptable value, the first point in the die to be exposed enters the illumination slit at t5t1. At t5t2, this first point on the die leaves the slit again. The stage-positioning errors in the interval 3t1, t2 4 determine the effect on overlay and imaging. Hence, the calculated MA and MSD values over this first interval correspond to the effect of

	positioning errors on the first point in the die. At t5t3, the last point of the die enters the slit, and, finally, at t5t4 the die leaves the slit again, making the interval 3t3, t4 4 the last window over which MA and MSD values need to be calculated. Hence, the total scan length of the stage equals the length of the die, plus the height of the slit, plus the length needed for settling of the stage. After t5t4, the stage decelerates again to standstill or follows another trajectory that brings the stage to the start of the next die." As a further example, "the ASML® TWINSCAN® NXE:3350B production-ready EVU system produces 125 computer wafers per hour using 13.5 nm wavelength light." *See* V. Marra, "ASML Advances Computing Breakthroughs with Multiphysics Modeling" at 4. As yet another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage:



See S. Miller, "Holistic View of Lithography for Double Patterning" (2009) at 25 ("**Holistic View of Lithography**"), ASML Sokudo Litho Breakfast Forum at 25, *available at* https://www.screen.co.jp/eng/spe/mt-images/SOKUDO_LBF2009_ASML.pdf (last visited June 15, 2021).

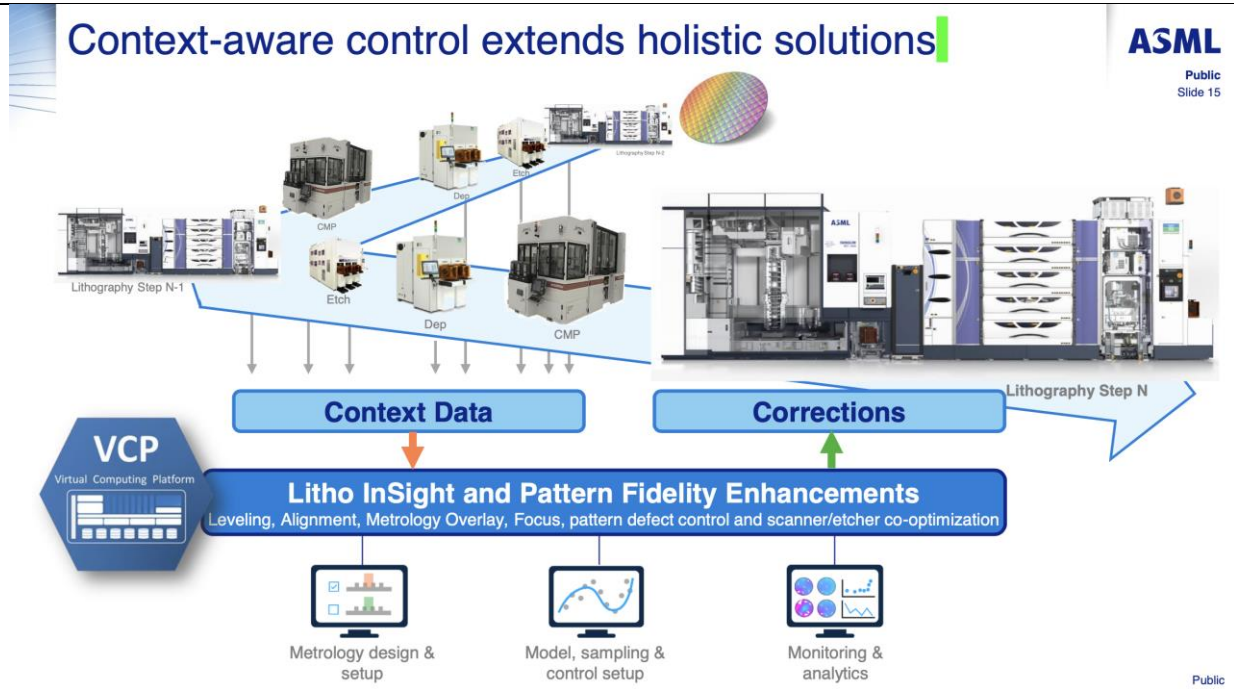
As a further example, the '651 Infringing Instrumentalities, including the TWINSCAN system, perform "Mask 1 Etch":



"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

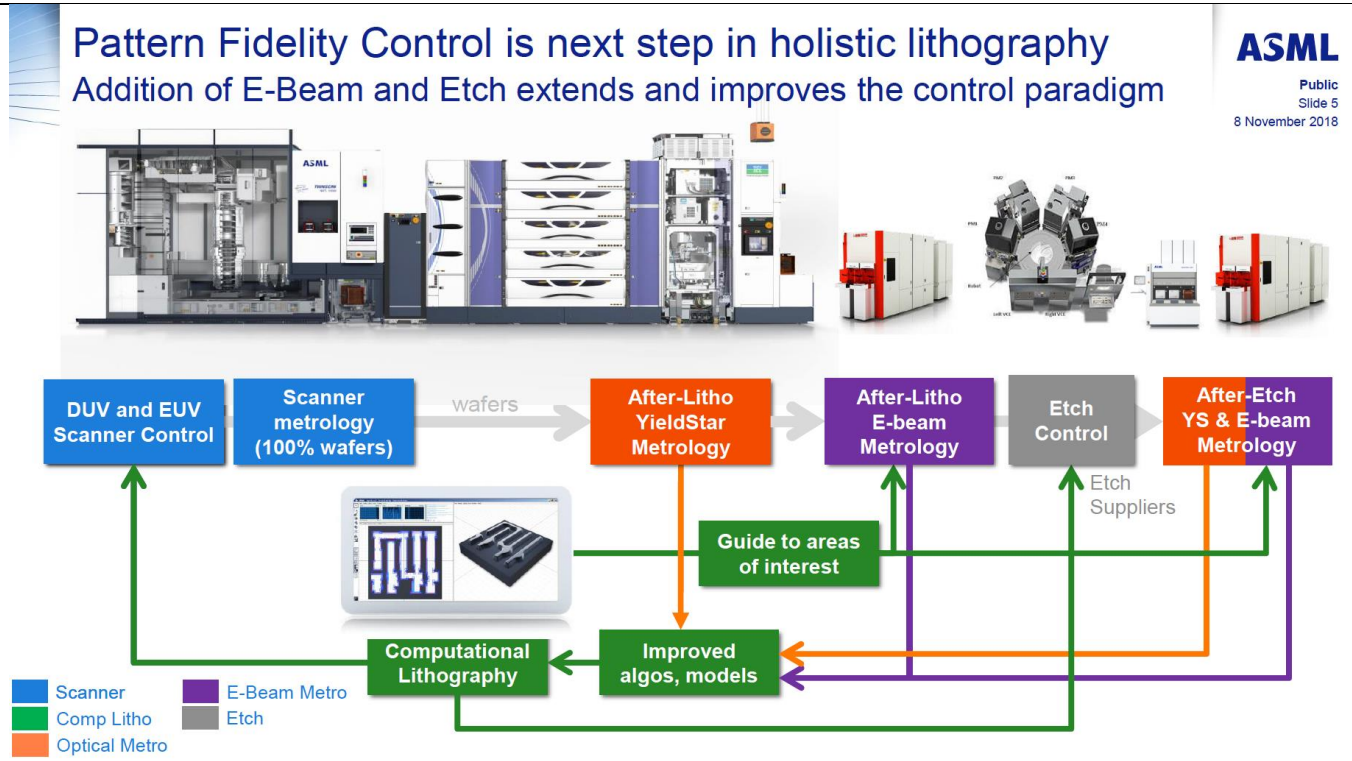
See K. Gorhad et al., "Co-optimization of RegC® and TWINSCANTM corrections to improve the intra-field on-product overlay performance" at Fig. 10 ("**Co-optimization of RegC® and TWINSCANTM Corrections**") *available at* https://www.semanticscholar.org/paper/Co-optimization-of-RegC-and-TWINSCAN-corrections-to-Gorhad-Sharoni/98d36fbae8f0d07a3051bcb3c29352db5ff172fc

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes:



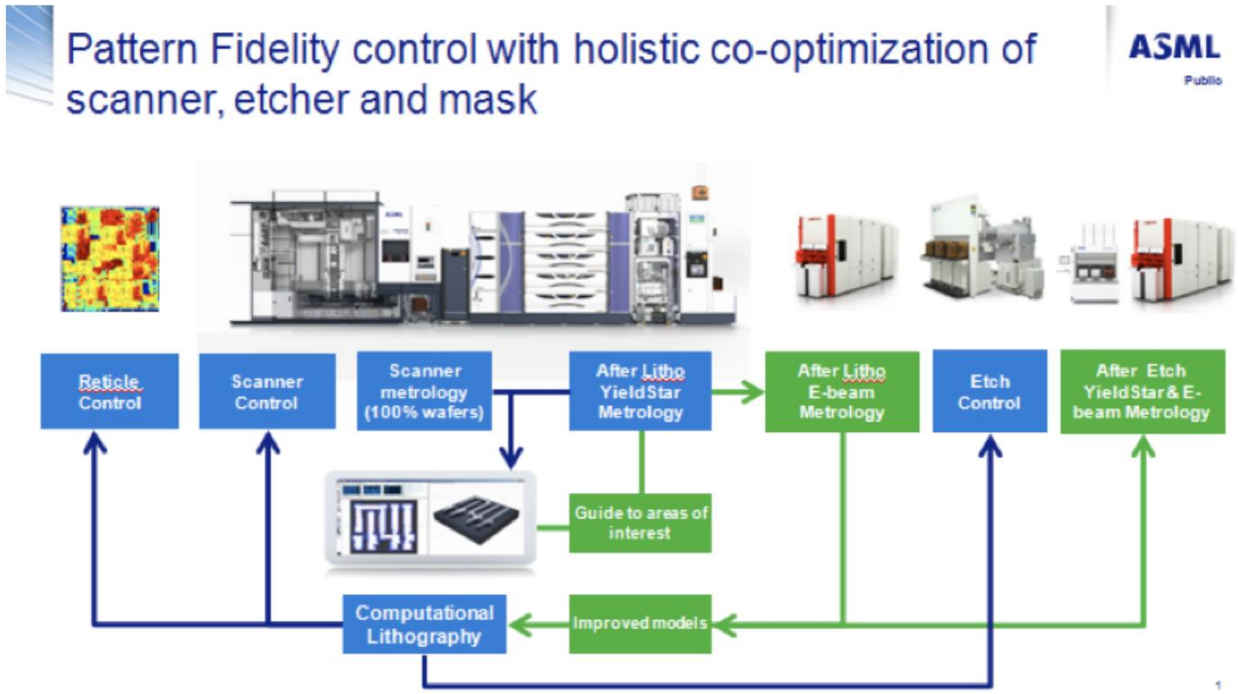
See Y. Cao, "Machine learning in computational lithography," ("**Machine Learning in Computational Lithography**") at 15 (2019), *available at* https://www.ebeam.org/docs/SPIE2019-yu-cao.pdf (last visited June 19, 2021).

As a further example, the '651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

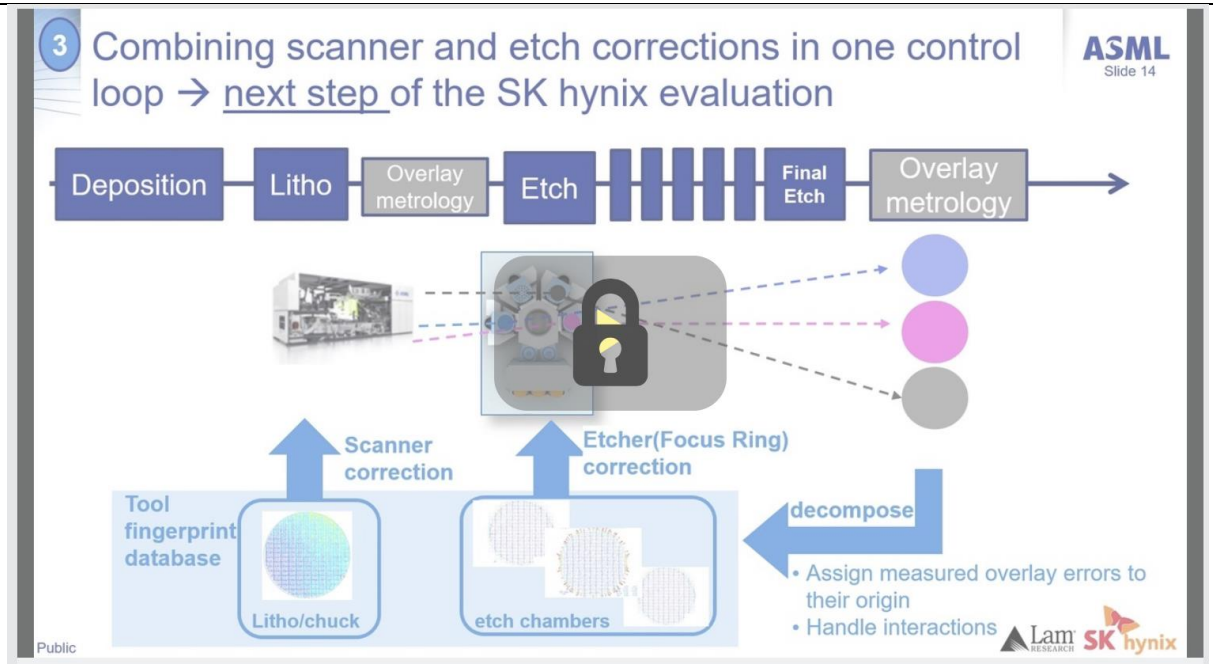
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:

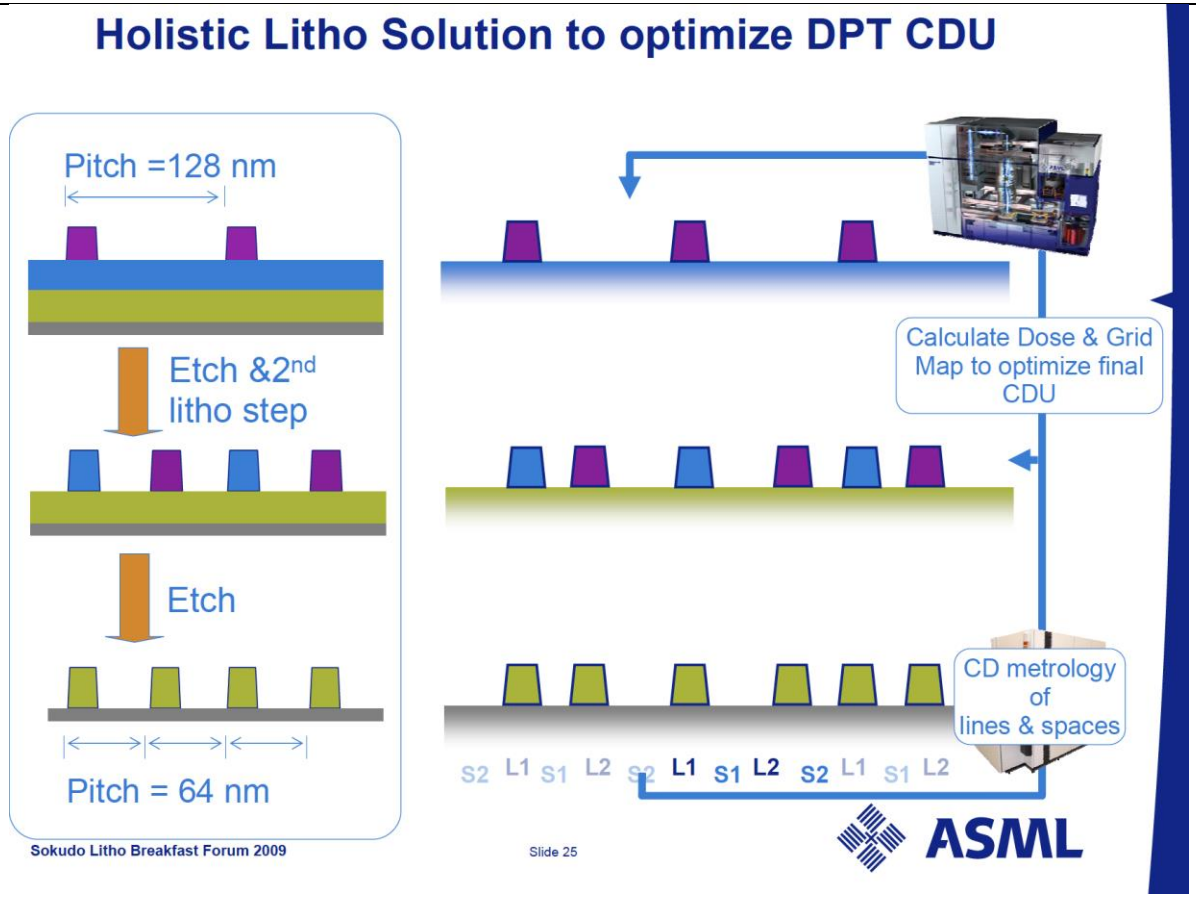


(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

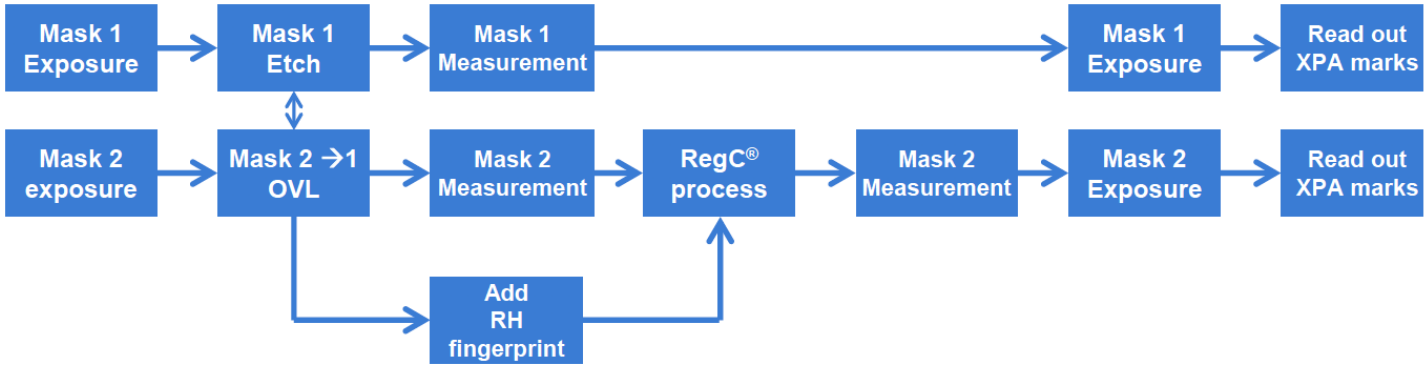
See Process Complexity at 2; *see also* Scanner and Etch Co-optimized Corrections (showing "combining scanner and etch corrections in one control"):

	
20. The method of claim 19, wherein providing a process chamber comprises providing at least one of a deposition chamber and an etching chamber.	The ’651 Infringing Instrumentalities comprise at least one of a deposition chamber and etching chamber. For example, the TWINSCAN system provides a process chamber that includes an etching chamber to perform etching:



See Holistic View of Lithography at 25.

As a further example, the '651 Infringing Instrumentalities, including the TWINSCAN system, perform "Mask 1 Etch," as shown below:



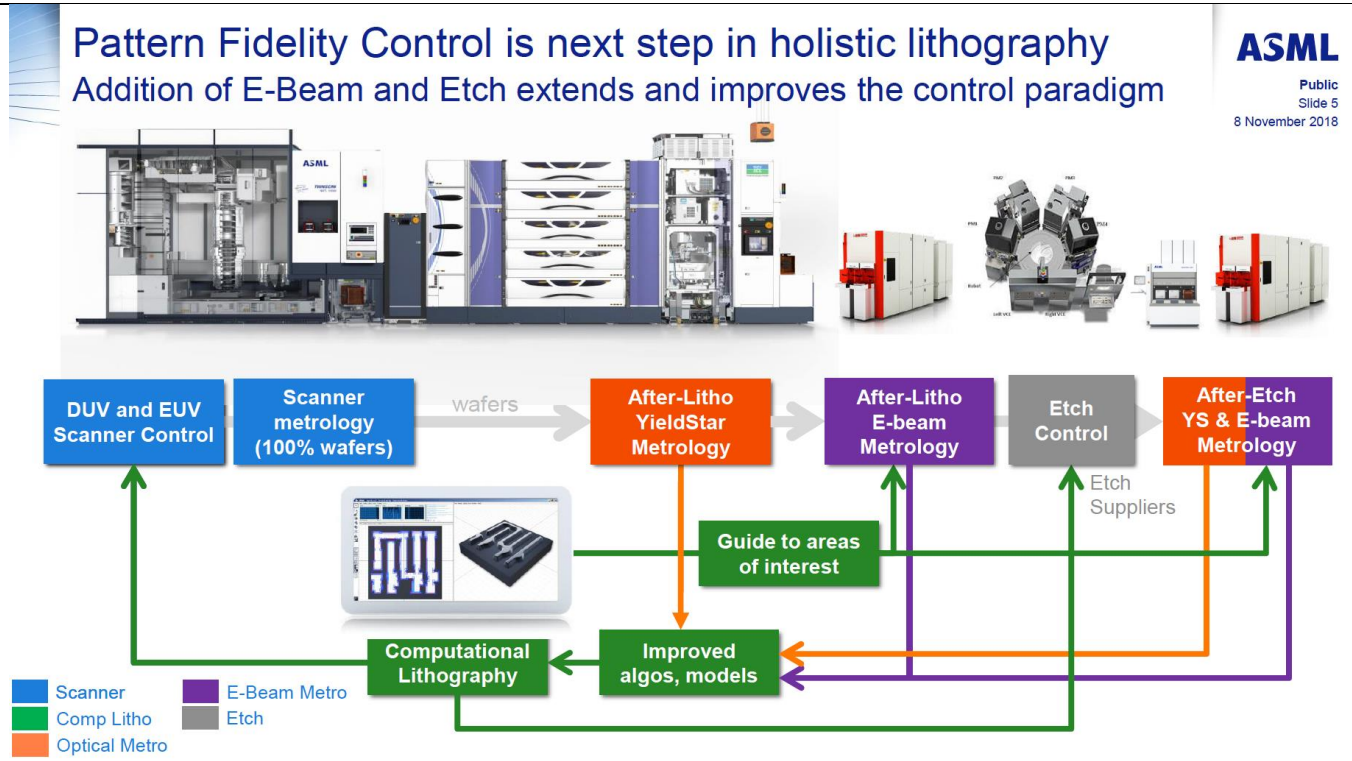
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes, as shown below:

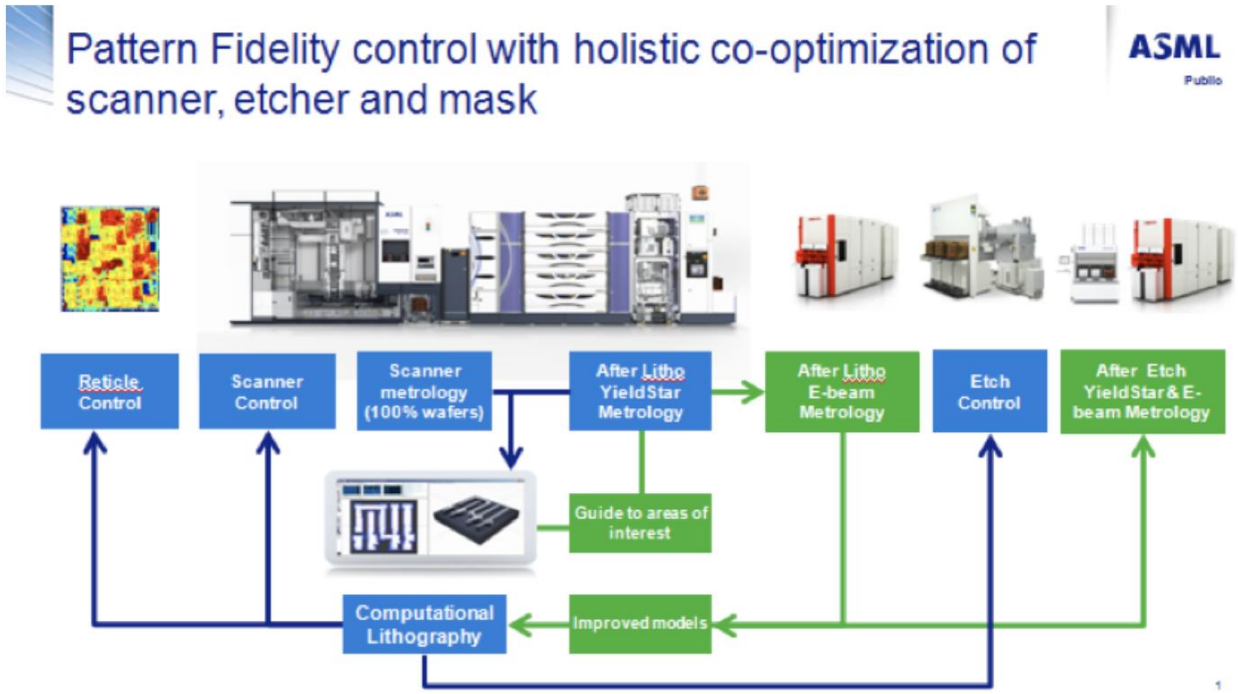
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

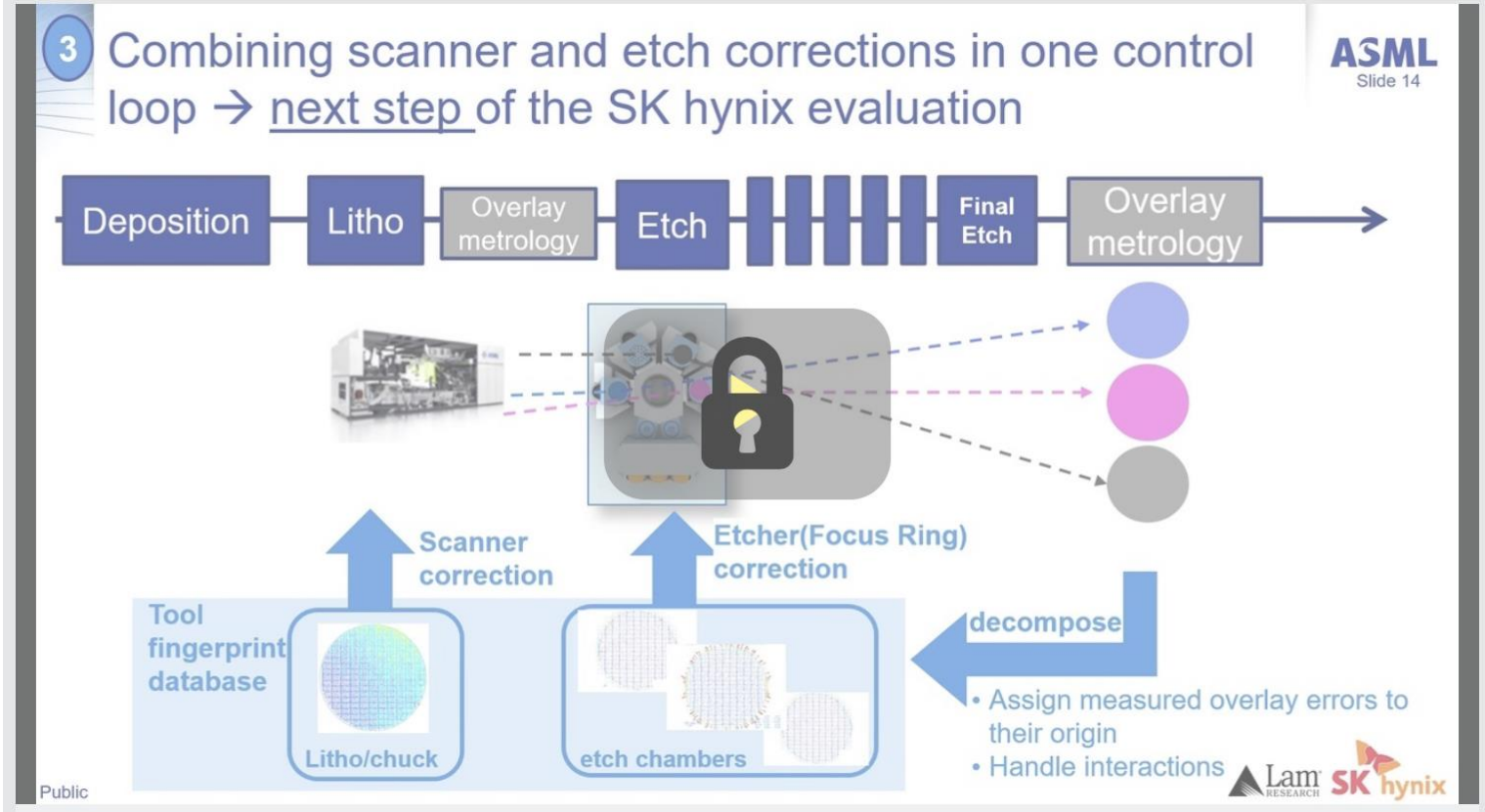
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:



(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

See P. Doe, "Process complexity means exponentially increasing data volumes and analysis challenges, with co-optimization across process steps," ("**Process Complexity**") at 2, *Semiconductor Digest* , *available at* https://sst.semiconductor-digest.com/2018/07/process-complexity-means-exponentially-increasing-data-volumes-and-analysis-challenges-with-co-optimization-across-process-steps/ (last visited June 19, 2021); *see also* I. Jeong *et al*., "Scanner and etch co-optimized corrections for better overlay and CD control" ("**Scanner and Etch Optimized Corrections**") (March 20, 2019), *available at* https://www.spiedigitallibrary.org/conference-proceedings-of-spie/10963/1096308/Scanner-and-etch-co-optimized-corrections-for-better-overlay-and/10.1117/12.2516578.short (last visited June 19, 2021) (showing "scanner and etch corrections in one control"):



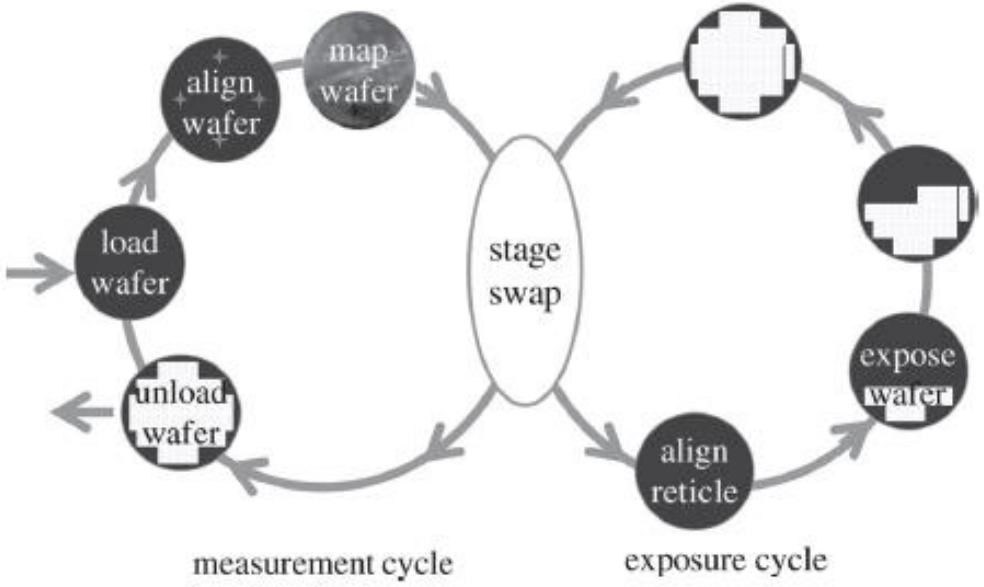
As a further example, the'651 Infringing Instrumentalities also include a chamber for deposition of pin-on-glass, anti-reflective coating and photoresist, as shown below:

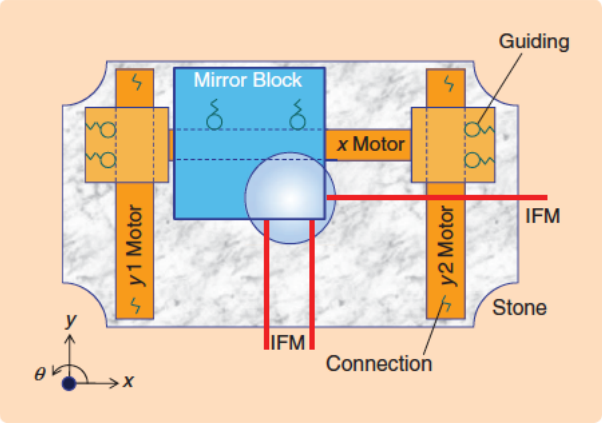
"Patterning was achieved by depositing 100nm SOC, 30nm spin-on-glass (SOG), 29nm Anti-Reflective Coating (ARC), and 105nm photoresist (PR) in an ASML Twinscan NXT:1950i 193nm immersion scanner, followed by lithographic patterning of line/space patterns."

See J. Soethoudt et al., "Defect mitigation in area-selective atomic layer deposition of ruthenium on titanium nitride/dielectric nanopatterns" ("Atomic Layer Deposition") at 8, *available at* https://lirias.kuleuven.be/2844955?limo=0 (last visited June 19, 2021).

21. The method of claim 19, wherein	The '651 Infringing Instrumentalities position a wafer on the wafer stage after the wafer stage has been adjusted. For example, the TWINSCAN system positions the wafer on the exposure table of the dual-wafer stage after the

positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage after said wafer stage has been adjusted.	exposure of a previous wafer is done and the exposure table is adjusted to receive a new wafer for the next cycle of exposure. *See, e.g.*, P. Drabik, "Performance prediction for Stage Positioning Measurement (SPM)," Master's Thesis, Eindhoven University of Technology, Department of Mathematics and Computer Science, *available at* https://pure.tue.nl/ws/files/72326295/Master_Thesis_Pawel_Drabik_Public.pdf ("Stage Positioning Management") at 1-2: "These systems are designed as wafer scanners which Performance prediction for Stage Positioning Measurement (SPM) 1 CHAPTER 1. INTRODUCTION perform the exposure process in step and scan fashion as presented in Figure 1.1. The reticle with circuit pattern is placed on a reticle stage (RS), whereas the silicon wafer is placed on a wafer stage (WS). During the scan movement the light is switched on with a desired dose and the exposure process starts. The stages move according to each other performing synchronized zig-zag movements. Next during the step movement the light is switched off, the reticle goes back to its initial position and the silicon wafer is prepared for exposure of a next die. The process repeats itself until all of the dies have been processed. Next, the reticle mask is replaced with a new one and the process can start all over again, exposing a new layer on top of the previous one. The exposure of consecutive layers needs to be done with nanometer precision in order to deliver highest quality circuits." Also, the exposure table is re-adjusted from the previous exposure before receiving the next wafer.
22. The method of claim 19, wherein positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage before said wafer stage has been adjusted.	The '651 Infringing Instrumentalities position a wafer on the wafer stage after said wafer stage has been adjusted. For example, the TWINSCAN system positions the wafer on the measurement table of the dual-wafer stage before the stage position of the measurement table is adjusted: "While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. T." *See* Position Control at 35. *See also* Stage Positioning Management at 3:

	 Figure 1.3: The process steps in TWINSCAN machine [18]
23. The method of claim 19, wherein performing a proces operation on said wafer comprises performing at least one of a deposition process and an etching proces in said process chamber.	The '651 Infringing Instrumentalities perform a proces operation on the wafer comprises performing at least one of a deposition process and an etching process in the process chamber. *See* Claim 20.
24. The method of claim 19, wherein adjusting said surface of said wafer stage	The '651 Infringing Instrumentalities adjust the surface of the wafer stage by actuating at least one of three pneumatic cylinders, each of which are operatively coupled to the wafer stage by a ball and socket connection. For example, each of the at least three pneumatic cylinders of the TWINSCAN system are operatively coupled to

comprises adjusting said surface of said wafer stage by actuating at least one of three pneumatic cylinders, each of which are operatively coupled to said wafer stage by a ball and socket connection.	the wafer stage via ball bearings:  FIGURE 5 Wafer stage top view. The wafer table is driven by three actuators, two of which drive the stage in the *y* direction and the remaining one in the *x* direction. The linear actuators also function as a guide for the horizontal motion, cooperating with ball bearings in the mover. The stage floats over a granite stone by means of an air bearing, and the linear actuators are connected to this stone as well. Interferometers measure the stage position, making use of mirroring side surfaces of the stage. *See* Position Control at 31 (annotated).
31. A method, comprising: performing a process operation in a process tool on each of a plurality of wafers;	The ’651 Infringing Instrumentalities perform a process operation in a process tool on each of a plurality of wafers. For example, the TWINSCAN system performs a process operation (e.g., lithography) in a process tool in each wafer:

See ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30, 2019).

The process chamber of the TWINSCAN system can be used for wafer exposure during lithography:

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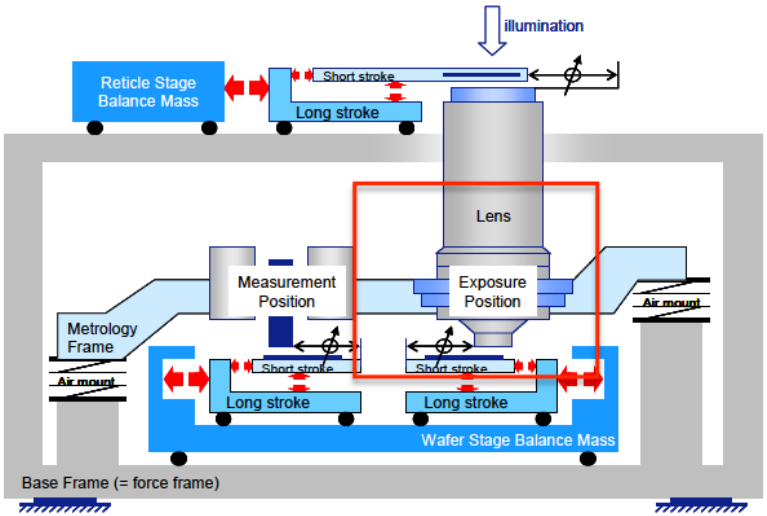


Figure 5. TWINSCAN™ dynamic architecture

See Perspective on Stage Dynamics and Control at 3 (annotated).

As a further example, TWINSCAN processes a plurality of wafers. For example, one of the measures of wafer scanner performance is throughput, which refers to “the number of wafers that are being exposed per hour.” See M.F. Heertjes, “Constrained iterative feedback tuning for robust control of a wafer stage system” (“Constrained Iterative Feedback Tuning”) at 4, available at https://pure.tue.nl/ws/files/7988078/713074251292725.pdf (last visited June 18, 2021).
</td>
</tr>
<tr>
<td>measuring a plurality of said processed wafers to determine across-wafer variations produced by said process operation performed in said process tool;</td>
<td>
The ’651 Infringing Instrumentalities measure a plurality of wafers to determine across-wafer variations produced by said process operation.

For example, the ’651 Infringing Instrumentalities measure a plurality of wafers to determine across-wafer variations, as shown below:

“Therefore the TWINSCAN™ dual stage system enables parallel measuring and exposing of a wafer as is schematically depicted in Figure 2.1. In the measurement position, a three-dimensional map of the wafer surface is generated using a high-spatial-frequency level sensor (ZLS). This wafer height map has a spatial resolution of 3.4-mm × 0.5-mm, which is obtained by using level sensor spots that have a dimension of 2.8-mm × 2.5-mm and over
</td>
</tr>
</table>

sampling in the scan direction. The high-resolution map of the wafer enables the optimization of the leveling profiles for the exposure slit size. The wafer map does not filter the height information needed to calculate the exposure slit size optimized leveling profiles, which is the way single stage leveling operates."

See M. Boonman et al., "The performance advantages of a dual stage system" ("**Performance Advantages of a Dual Stage System**"), Proc. of SPIE vol. 5377 (2004) at 743-44.

See also id. at Fig. 2.1:

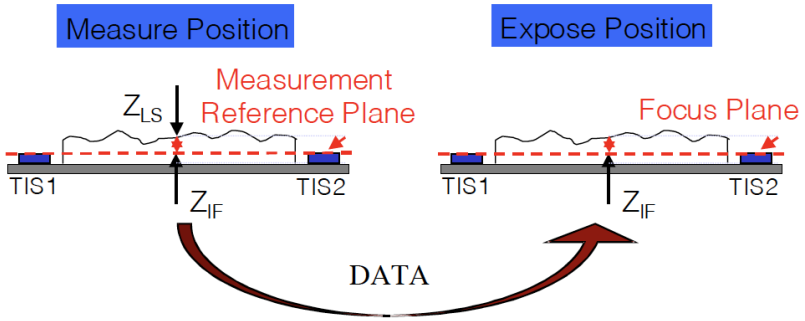


Figure 2.1: *Principle of the dual stage leveling technology: using a level sensor to measure the wafer map with respect to the measurement reference plane connected to TIS fiducials.*

See also id. at 745-46:

"3.1 Interfield height variation: Topography versus flat wafers
To prove the focus performance advantage of a dual stage system compared to a single stage system, Leveling Qualification Tests and full wafer CD uniformity exposures are performed. In this experiment we used checkerboard wafers along with ultraflat wafers. A complete wafer height map is determined by scanning the complete wafer underneath the sensor in a pattern corresponding to the exposure fields. Figure 3.1 (a) gives an example of a measured wafer map of a checkerboard that has alternating etched fields of about 300 nm deep."

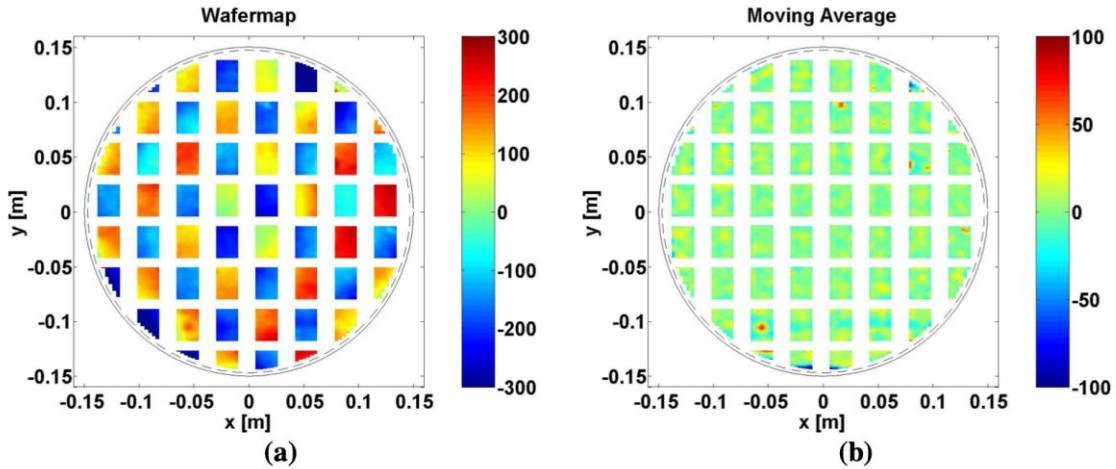


Figure 3.1: (a) Measured wafer map of a 300 mm checkerboard wafer, (b) Leveling calculations showing the wafer non- correctable error MA(z) of the same wafer.

The checkerboard wafer has up to 300nm height differences between fields (etched down into the wafer). In a dual stage scanner the exposure profiles are determined based on the measured height of the fields to be exposed, and are not influenced by the height of any neighbouring field due to the look-ahead functionality. While in a single stage system the settling scan trajectory is based on on-the-fly measurements, in a dual stage system this is based on extrapolating the exposure profiles calculated from the measured wafer height map before exposure.
In figure 3.1 (b), the non-correctable errors MA(z) of the checkerboard wafer are presented. These wafer MA(z) results show the same response as for an ultra flat wafer meaning that the leveling system can accurately compensate the height differences in this wafer. On exposure therefore there will be no difference up to the leveling optimization whether an ultra flat or wafer with topography is used. The system will automatically level the wafer surface to the focal plane of the lens. This is proven by exposing a LQT on this wafer, which results are shown in figure 3.2 (a). Figure 3.2 (b) shows the results of the full wafer CDU exposure.

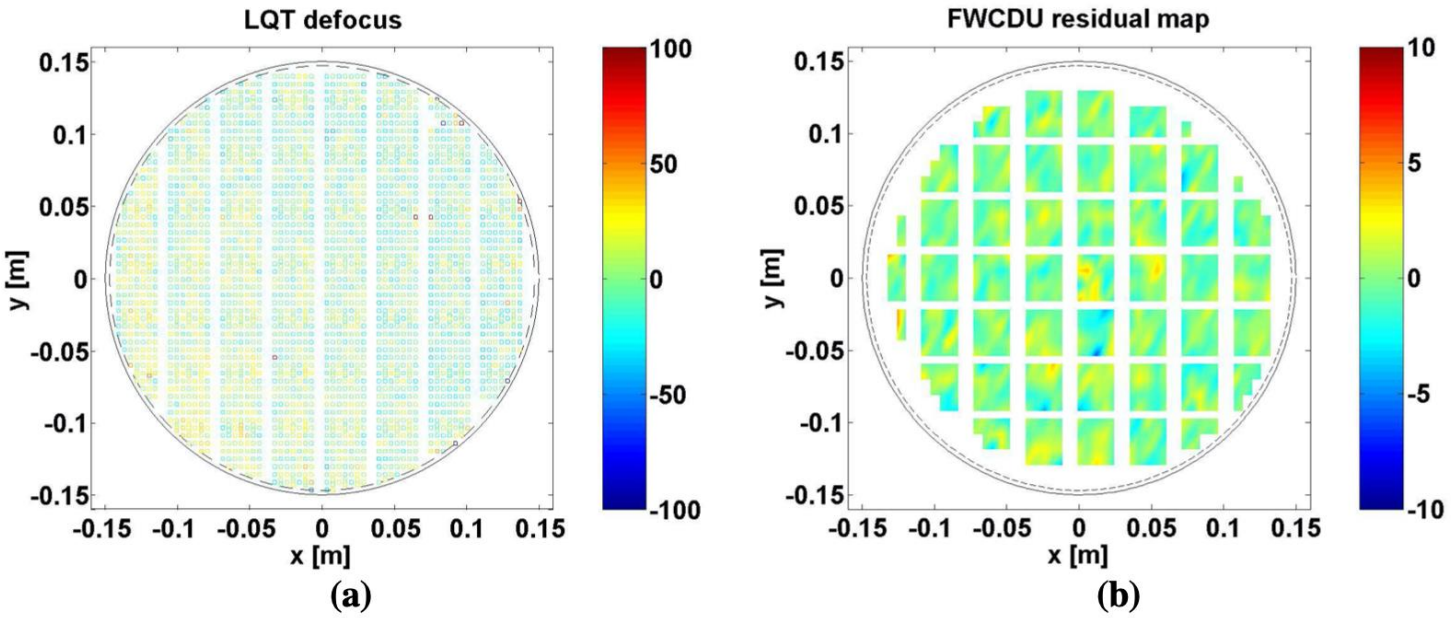


Figure 3.2: (a) Leveling Qualification Test (LQT) results of checkerboard wafer, and (b) FWCDU results of checkerboard wafer with mathematically removed inter field CD finger print, resulting in FWCDU = 5.1 nm 3σ for 100nm Isolated lines.

See also id. at 747-48:

"3.2 Intrafield height variation: Inner field characteristics
Besides the artificially created topography wafer with interfield height variation, a set of 20 different wafers is used for leveling performance qualification of single and dual stage systems. These 20 wafers comprise Double Side Polished wafers (DSP), Single Side Polished wafers (SSP) and a variety of processed wafers (Processed), Front-end, Back-end and some focus challenging wafers with different topography. These 20 wafers are split in two batches of 10 each, which have been used for the experiments. The LQT reticle (used to measure leveling performance) was exposed on the first set of 10 wafers using a field size of 26mm wide and 32mm long. The second set of 10 wafers was exposed using a typical fieldsize of 20mm wide and 32mm long. Both sets of wafers were exposed under identical exposure conditions such as resist, wavelength, NA, etc. Full wafer coverage exposures were done, but first we concentrate on the inner fields (edge fields discussed in section 4)."

"All 20 wafers were used for leveling qualification of different systems: 1) single stage scanner using on-the-fly leveling technology with a multi spot level sensor, 2) two different possible improvements (a) and (b) of single stage leveling concepts (look-ahead improvements), and 3) the dual stage leveling system. The exposure test conditions over all systems were taken identical. Besides the experimental focus qualification, the theoretical defocus prediction based on the intrinsic wafer flatness and the finite exposure slit size, the wafer MA(z) is plotted (wafer). These non-correctable errors were calculated using measured wafer maps on dual and single stage systems and taking the average for the two systems, taking into account the possible differences in clamping between the different scanner types. The defocus distribution over all points on inner fields on the wafers is characterized by its sigma value.

Figures 3.4 and 3.5 show the leveling performance in 3 sigma defocus results of the LQT exposures. The data is sorted per wafer, with increasing wafer roughness along the horizontal axis. Per wafer the different systems are compared. Figure 3.4 shows the results of set 1; figure 3.5 of set 2."

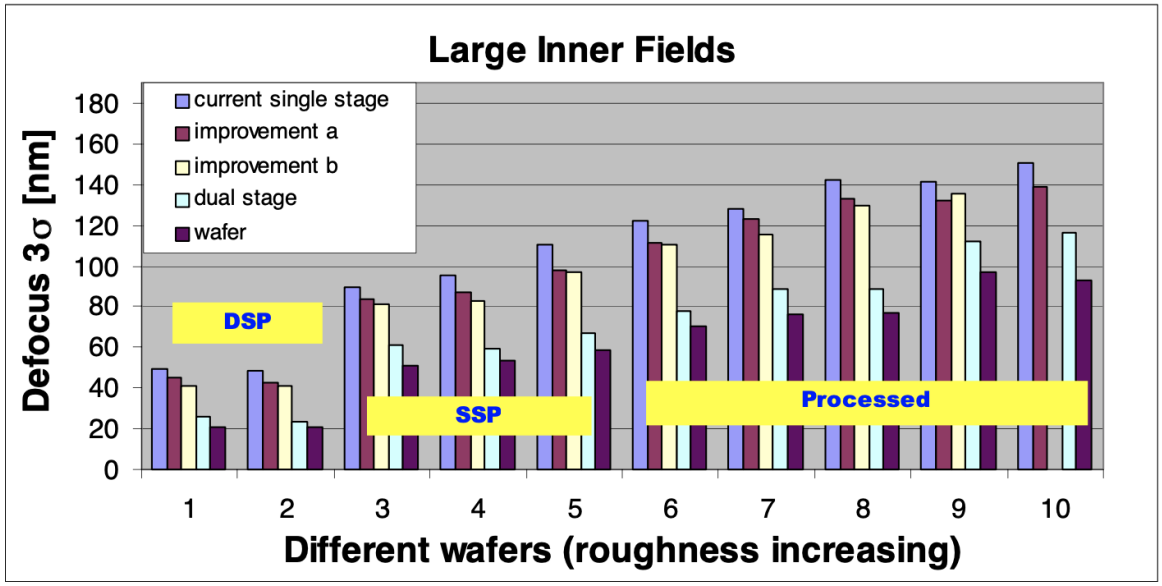


Figure 3.4: Focus performance on a set of 10 different wafers increasing in roughness. Different scanning leveling technologies are compared on large inner fields. The theoretical best achievable values are plotted as reference (wafer).

"The comparison of defocus in figure 3.4 clearly shows the focus performance advantage of a dual stage system with respect to the single stage systems. On all different wafers, the dual stage system outperforms a single stage

system. Comparing the dual stage system experimental focus performance with the theoretical best achievable values based on the measured wafer maps given the intrinsic wafer flatness and finite slit size, shows that the total focus performance is having its major contribution from the intrinsic wafer flatness. The dual stage system comes closest to this ideal performance and adds only a small contribution to the total defocus."

See also Stage Positioning Management at 19:

"3.1 SPM in position control Stage Position Measurement (SPM) is a part of a position control system in ASML lithoscanners. Its essential function is to measure position of the stages (WS or RS) relative to a metrology frame and distribute in real-time to other systems at synchronized moments of time. The calculated stage position is given in 6DoF coordinate system (X, Y, Z, Rx, Ry and Rz) [9]. Figure 3.1 presents a position control system of a WS/RS with closed control loop pattern, where the SPM system has been marked with a red block. As can be seen the SPM receives data from the Position Sensors, next processes the data and passes the outcome to the position control of the stages."

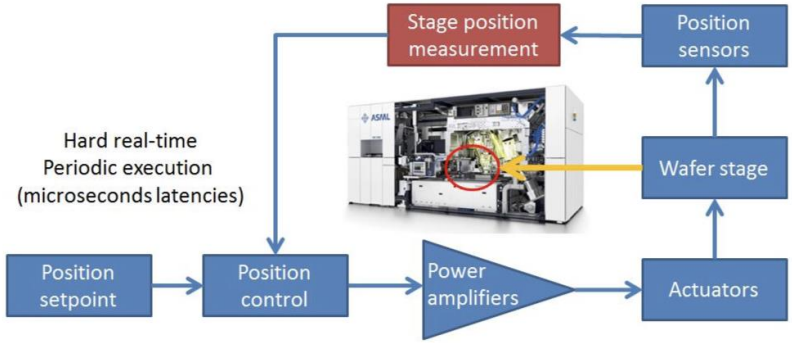


Figure 3.1: Closed loop position control of Wafer Stage with Stage Position Measurement

Also, upon information and belief, the '651 Infringing Instrumentalities obtain surface level measurements of a wafer at a plurality of different level sensing locations across the substrate as part of the exposure process. For example, in one of ASML's own patents, USP No. 8,908,148, it is disclosed that its system is configured to perform "obtaining a plurality of surface level measurements of a substrate at a plurality of different level sensing locations across the substrate . . . ." *See* 2:19-21.

As another example, the '651 Infringing Instrumentalities, including ASML's YieldStar system, perform measurement of wafers to determine across-wafer variations including, for example, overlay and critical dimension:

"The S-100 can handle up to 90 WpH measured with a sample plan of 3 densely measured wafers (36 CD and 36 overlay points) and 22 less-densely measured wafers (5 CD and 5 overlay points). The S-200 and T-200 can handle up to 150 WpH, which means it is roughly 67% faster. Another improvement is that most specifications are tightened."

J. Maas et al., "YieldStar: a new metrolog platform for advanced lithography control," Proceedings of SPIE, 27th Eurpean Mask and Lithography Conference, Dresden Germany (2011), at 4; *see also id.* at Fig. 6:

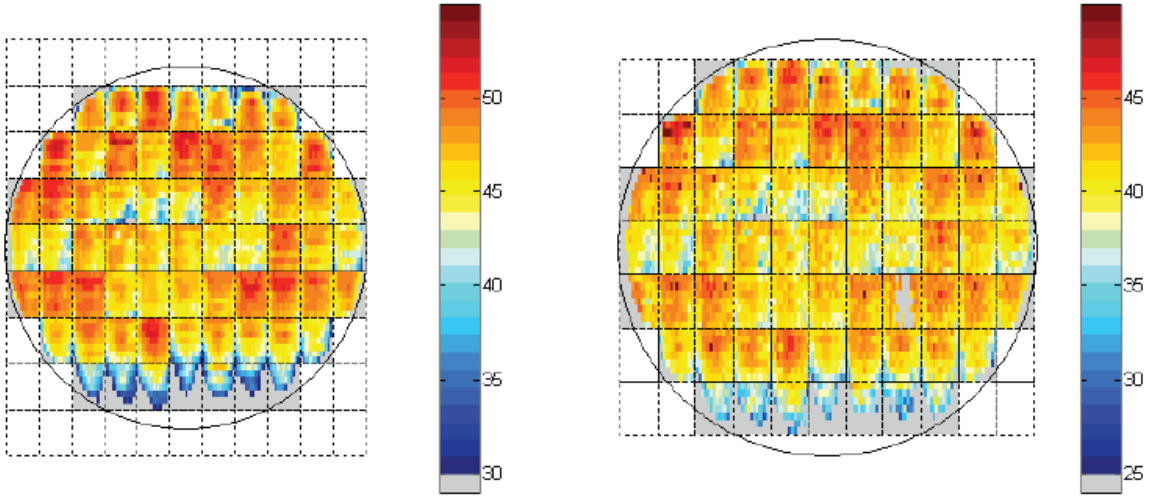


Figure 6. Wafer map data collected with YieldStar (left) and CD-SEM (right) show similar signature.

See also ASML, "Lithography Principles, Measuring Accuracy," *available at* https://www.asml.com/en/technology/lithography-principles/measuring-accuracy (last visited Apr. 30, 2020):

"Fast, accurate wafer metrology In wafer metrology, key manufacturing parameters such as overlay (the accuracy

	with which two layers of a chip are aligned) and focus (how sharp the image is) are monitored by measuring how well a particular repeating pattern (the 'metrology target') is printed on the wafer. These measurements are made at marked locations across the wafer. . . . Metrology data is analyzed in control software and fed back to the lithography system in real-time, which enables customers to tune the manufacturing process further for optimal yield."
adjusting, based upon said measured across-wafer variations, a plane of a surface of an adjustable wafer stage; and	The '651 Infringing Instrumentalities adjust a plane of a surface of an adjustable wafer stage based upon measured across-wafer variations: For example, the TWINSCAN system adjusts the plane of the wafer stage based upon across-wafer variations, as shown below: "However, during a scanned exposure, the non-correctable errors change continuously as the slit is scanned over a particular position on the wafer. In the latter case, the average value of the non-correctable errors over the exposure time defines the average defocus that this position experiences during the exposure. We define the value that depends on the slit size and on the spatial-frequency and amplitude of the wafer topography as simulated defocus, or as the Moving Average in the z-direction (MA(z)). Changes in the topography that are larger then the slit dimensions can be leveled by adjusting the stage height and tilt angle accordingly." *See* Performance Advantages of a Dual Stage System at 743-44. As another example, the TWINSCAN system makes adjustments to the lithography process as shown below:

See Machine Learning in Computational Lithography at 15.

See also Constrained Iterative Feedback Tuning at 3, available at https://www.semanticscholar.org/paper/Constrained-Iterative-Feedback-Tuning-for-Robust-of-Heertjes-Velden/99b6e89728a28f9c23e8eaa35dcc78fe09061824 (last visited Feb. 9, 2021):

"**Remark 2** The wafer stage system is a multivariable sys-tem that through a proper choice of input/output decoupling matrices becomes diagonally dominant. Multi-input multi-output (MIMO) stage control is therefore often done with adiagonal controller structure in the six degrees-of-freedom:x,y,rz,z,rx,ry. For clarity of presentation, only the scanning y-direction is subject to further (constrained) IFT optimization, see [16], [17], [35] for examples of MIMO IFT and[33], [45] for MIMO model-based counterparts."

See also Performance Advantages of a Dual Stage System at 744:

"In Figure 2.2 the different performance indicators used in this paper are described. Scanner "leveling performance" relates to how well the scanner is capable to position wafer surface in a flat plane that is coupled to the focal plane

position of the projection lens. This leveling performance can be separated into two different contributions, a leveling contribution and a servo system contribution. The latter error is the deviation of the position of the stage compared to the requested position by the leveling system. The leveling contribution includes errors from the level sensor, the eventually needed additional filtering and the wafer non-correctables."

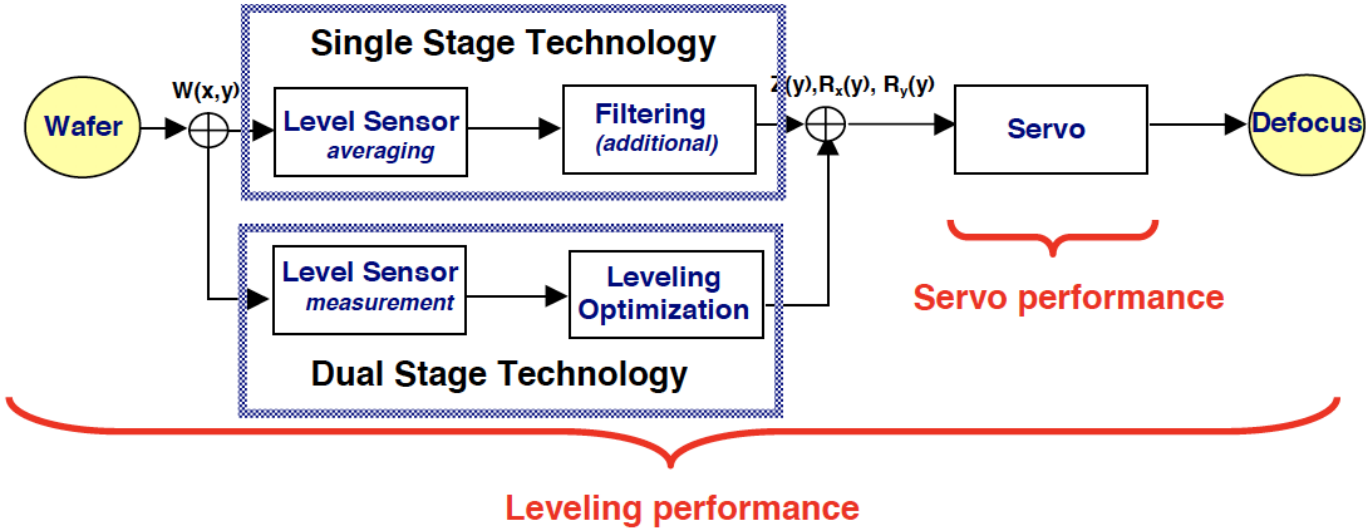


Figure 2.2: *Schematic representation of the focus operation in scanning exposure systems and the different performance indicators as used throughout this paper. Dual versus Single stage leveling operations are shown as separate paths.*

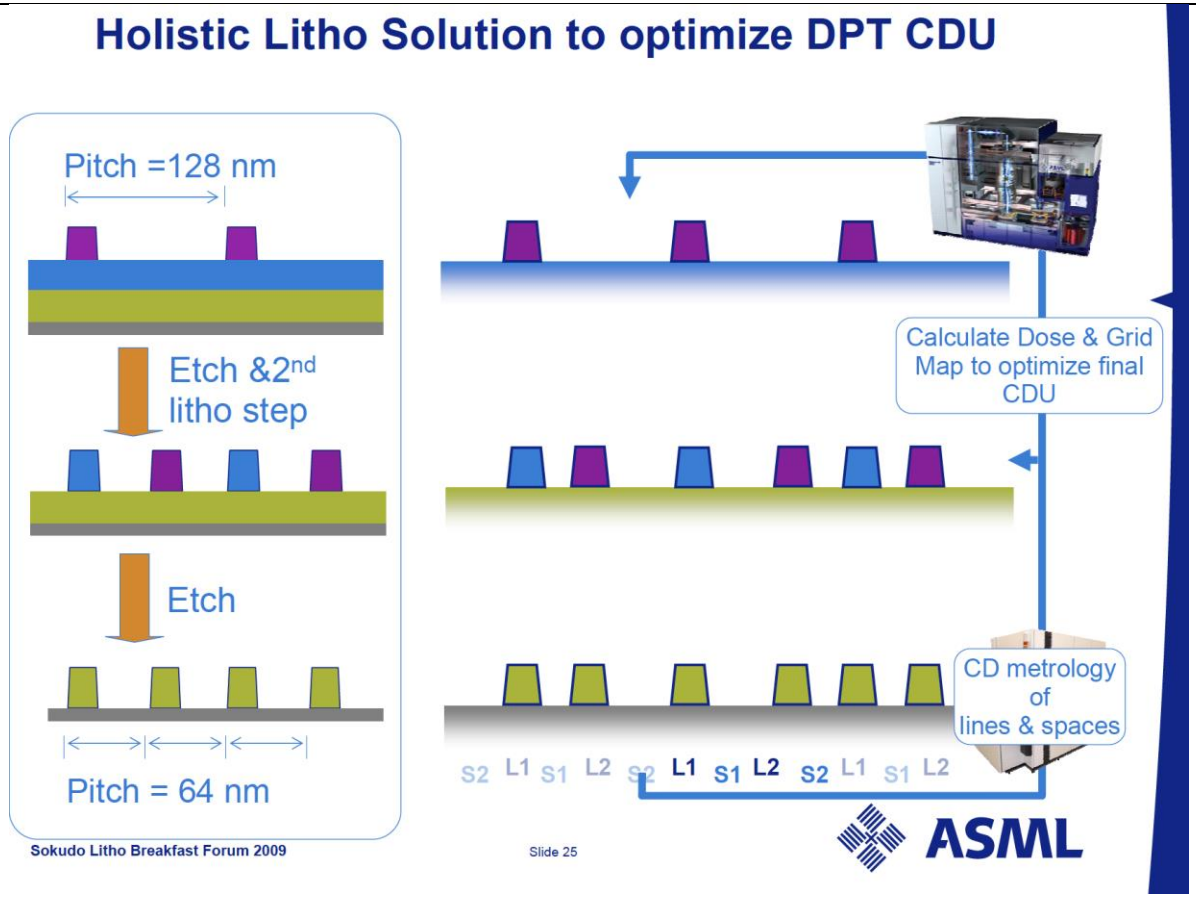
As yet another example, the measured across-wafer variations (e.g., metrology data) are used to adjust a plane of a surface of the wafer stage by making corrections to the scale and height maps:

"The WS Position Measurement System uses four 3D encoders. Each of the encoder delivers the 3D position of the encoder. The metrology model implements the algorithm for conversion of the encoders signals into 6DoF."

See Stage Positioning Management at 21; *see also id.* at 22:

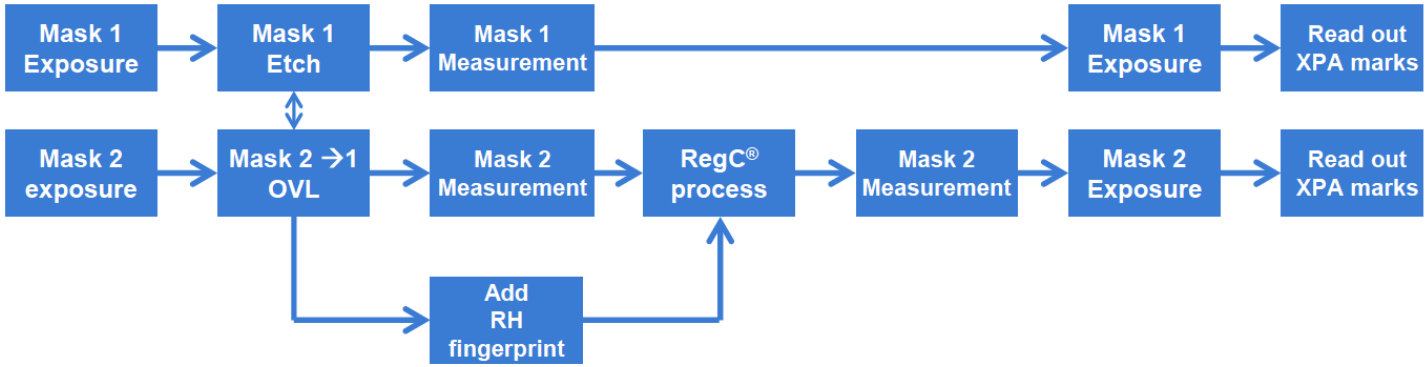
	<table><tr><th>Number</th><th>Task</th></tr><tr><td>1</td><td>Conversion to bits and meters</td></tr><tr><td>2</td><td>Conversion to rotation coordinates</td></tr><tr><td>3</td><td>Determine sensor weights</td></tr><tr><td>4</td><td>Global transformation model</td></tr><tr><td>5</td><td>Delay corrections</td></tr><tr><td>6</td><td>Scale and height maps corrections</td></tr><tr><td>7</td><td>Calculation of linear model coefficients</td></tr></table> Table 3.2: Tasks performed during NTC calculation phase for SPM RS [8] *See also* ASML, "Lithography Principles, Measuring Accuracy," *available at* *https://www.asml.com/en/technology/lithography-principles/measuring-accuracy* (last visited Apr. 30, 2020): "Fast, accurate wafer metrology In wafer metrology, key manufacturing parameters such as overlay (the accuracy with which two layers of a chip are aligned) and focus (how sharp the image is) are monitored by measuring how well a particular repeating pattern (the 'metrology target') is printed on the wafer. These measurements are made at marked locations across the wafer. . . . Metrology data is analyzed in control software and fed back to the lithography system in real-time, which enables customers to tune the manufacturing process further for optimal yield."
performing said process operation on at least one subsequently processed wafer positioned on said wafer stage in said process chamber after said plane of said wafer stage has been adjusted.	The '651 Infringing Instrumentalities perform the process operation on at least one subsequently processed wafer positioned on the wafer stage in said process chamber after the plane of the wafer stage has been adjusted. For example, the TWINSCAN system performs the process operation on at least one subsequently processed wafer positioned on the wafer stage in said process chamber after the plane of the wafer stage has been adjusted, as shown below: "A solution was found by equipping the system with two wafer stages [7]. While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure.

	When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. The increased stage acceleration and speed further improves throughput." *See* Position Control at 39-40; *see also id*. at 37: "Figure 16 shows a more detailed timing diagram of the stage movement during a scan. Figure 16(b) shows an acceleration setpoint profile, which in this example is a thirdorder profile instead of the previously used second-order profile. Figure 16(a) shows the velocity setpoint profile. At t5t0, the acceleration phase ends, and a constant velocity is reached. After a certain settling time, which allows the remaining controller error to be reduced to an acceptable value, the first point in the die to be exposed enters the illumination slit at t5t1. At t5t2, this first point on the die leaves the slit again. The stage-positioning errors in the interval 3t1, t2 4 determine the effect on overlay and imaging. Hence, the calculated MA and MSD values over this first interval correspond to the effect of positioning errors on the first point in the die. At t5t3, the last point of the die enters the slit, and, finally, at t5t4 the die leaves the slit again, making the interval 3t3, t4 4 the last window over which MA and MSD values need to be calculated. Hence, the total scan length of the stage equals the length of the die, plus the height of the slit, plus the length needed for settling of the stage. After t5t4, the stage decelerates again to standstill or follows another trajectory that brings the stage to the start of the next die." As a further example, "the ASML® TWINSCAN® NXE:3350B production-ready EVU system produces 125 computer wafers per hour using 13.5 nm wavelength light." *See* V. Marra, "ASML Advances Computing Breakthroughs with Multiphysics Modeling" at 4. As yet another example, the TWINSCAN performs a process operation (e.g., lithography and/or etching) on at least one substequently processed wafer positioned on the wafer stage in the process chamber after the plane of the wafer stsage has been adjusted:



See Holistic View of Lithography at 25.

As a further example, the ’651 Infringing Instrumentalities, including the TWINSCAN system, perform “Mask 1 Etch” on at least one substequently processed wafer positioned on the wafer stage in the process chamber after the plane of the wafer stsage has been adjusted:



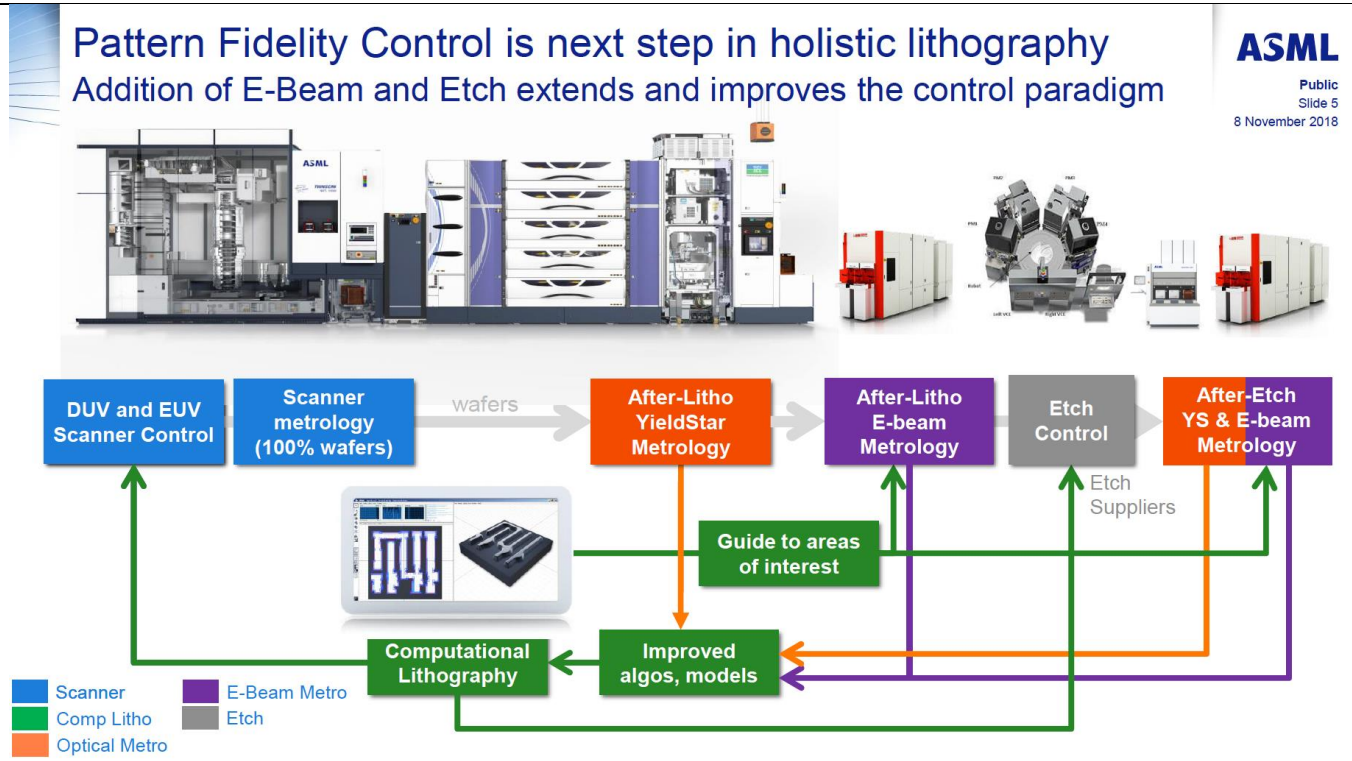
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM Corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes on at least one substequently processed wafer positioned on the wafer stage in the process chamber after the plane of the wafer stsage has been adjusted:

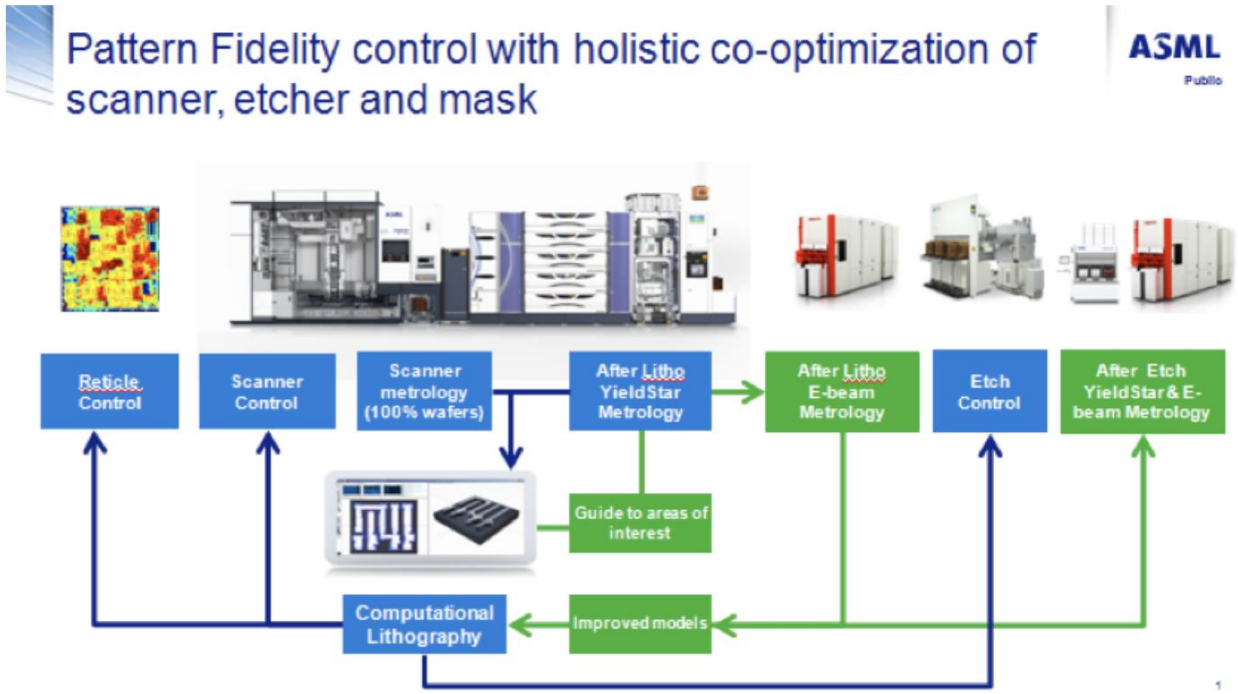
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

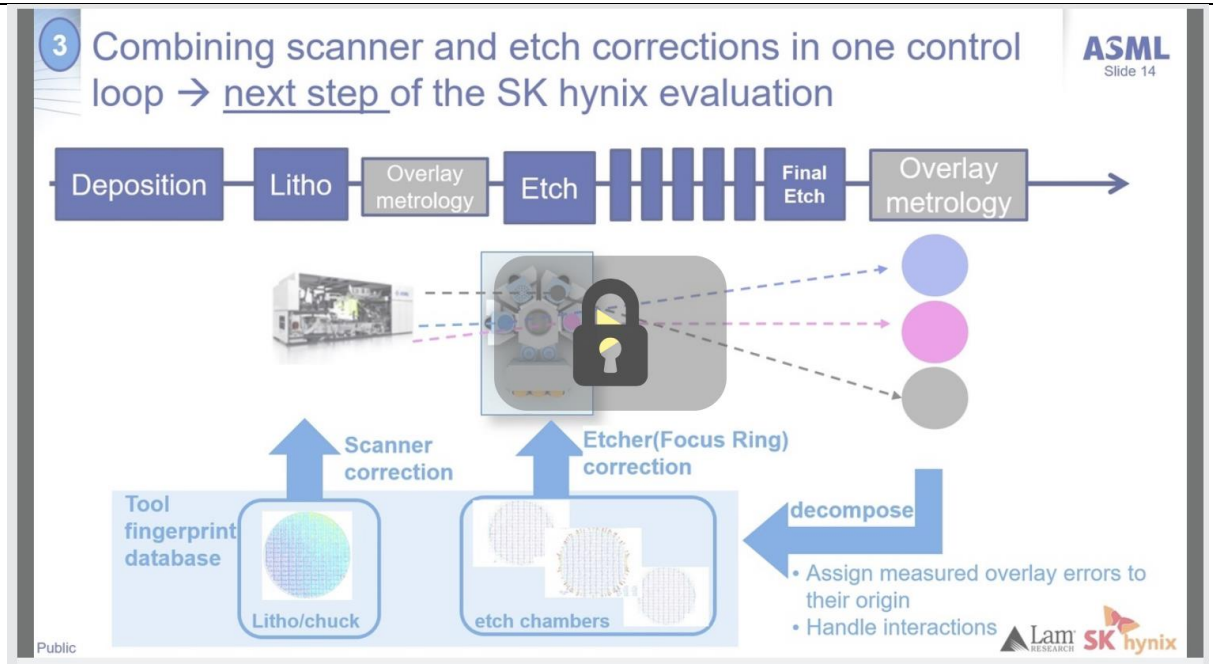
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:

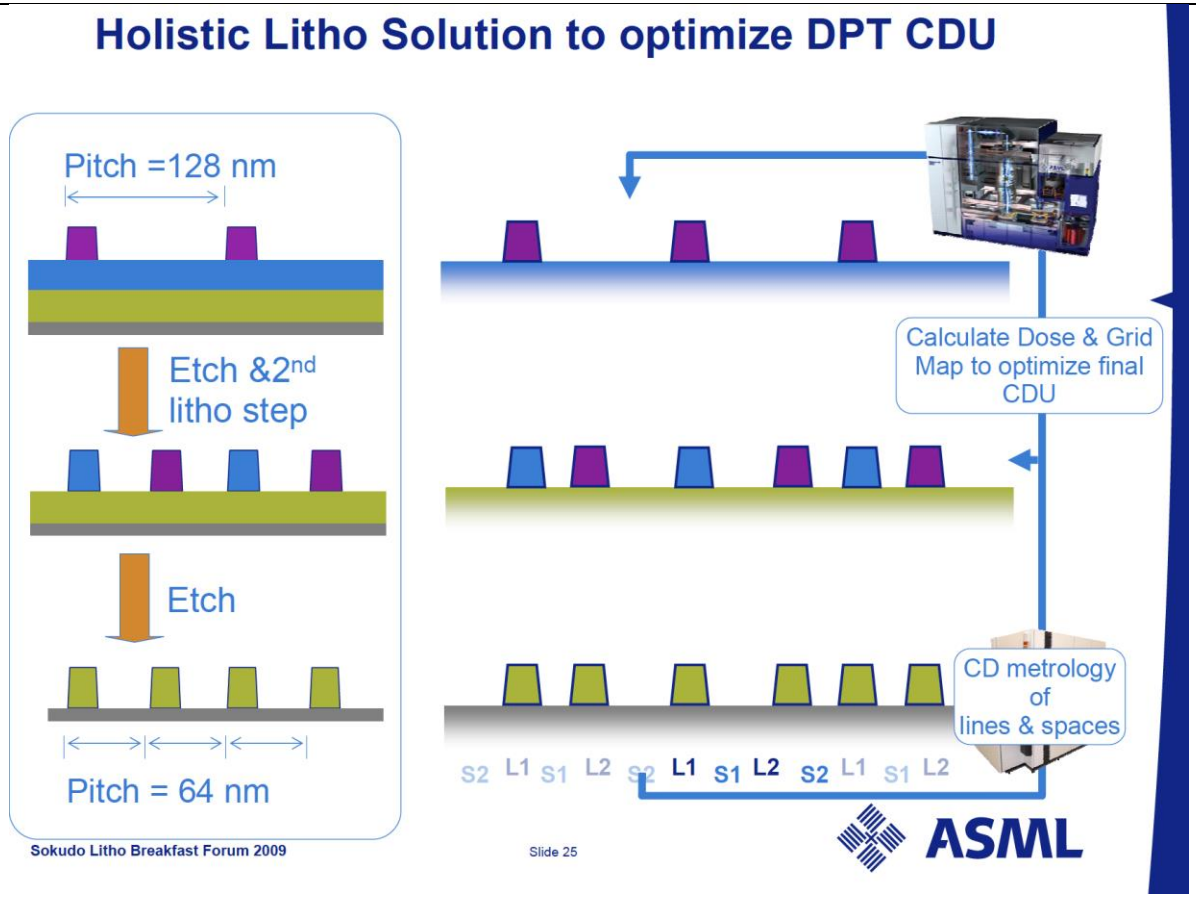


(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

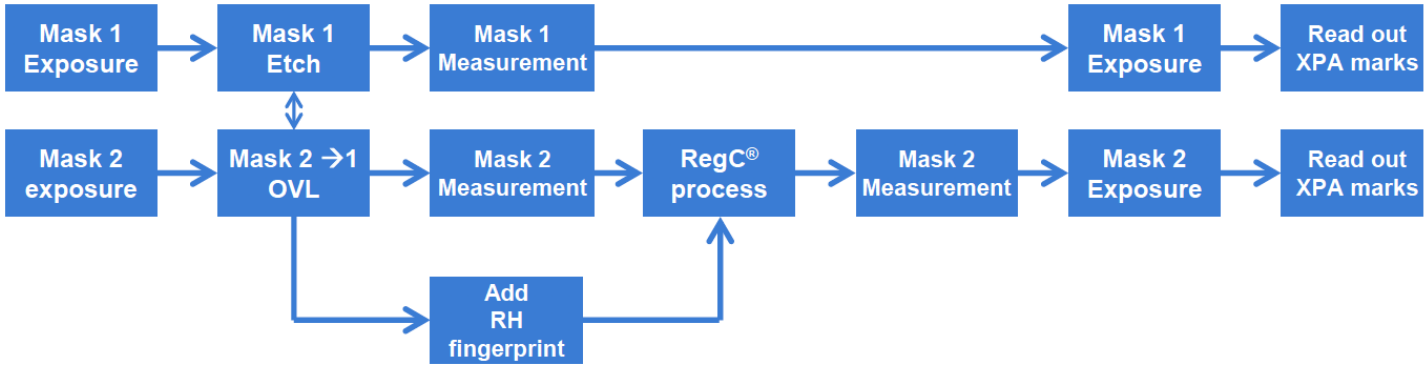
See Process Complexity at 2; *see also* Scanner and Etch Co-optimized Corrections (showing "combining scanner and etch corrections in one control"):

	
32. The method of claim 31, wherein performing a process operation in a process tool on each of a plurality of wafers comprises performing a process operation comprised of at least one of a deposition process and an etching process in a process tool on each of a plurality of wafers.	The ’651 Infringing Instrumentalities perform a process operation comprised of at least one of a deposition process and an etching process in a process tool on each of a plurality of wafers. For example, the TWINSCAN system performs a process operation comprised of at least one of a deposition process and an etching process in a process tool on each of a plurality of wafers, as shown below:



See Holistic View of Lithography at 25.

As a further example, the '651 Infringing Instrumentalities, including the TWINSCAN system, perform "Mask 1 Etch," as shown below:



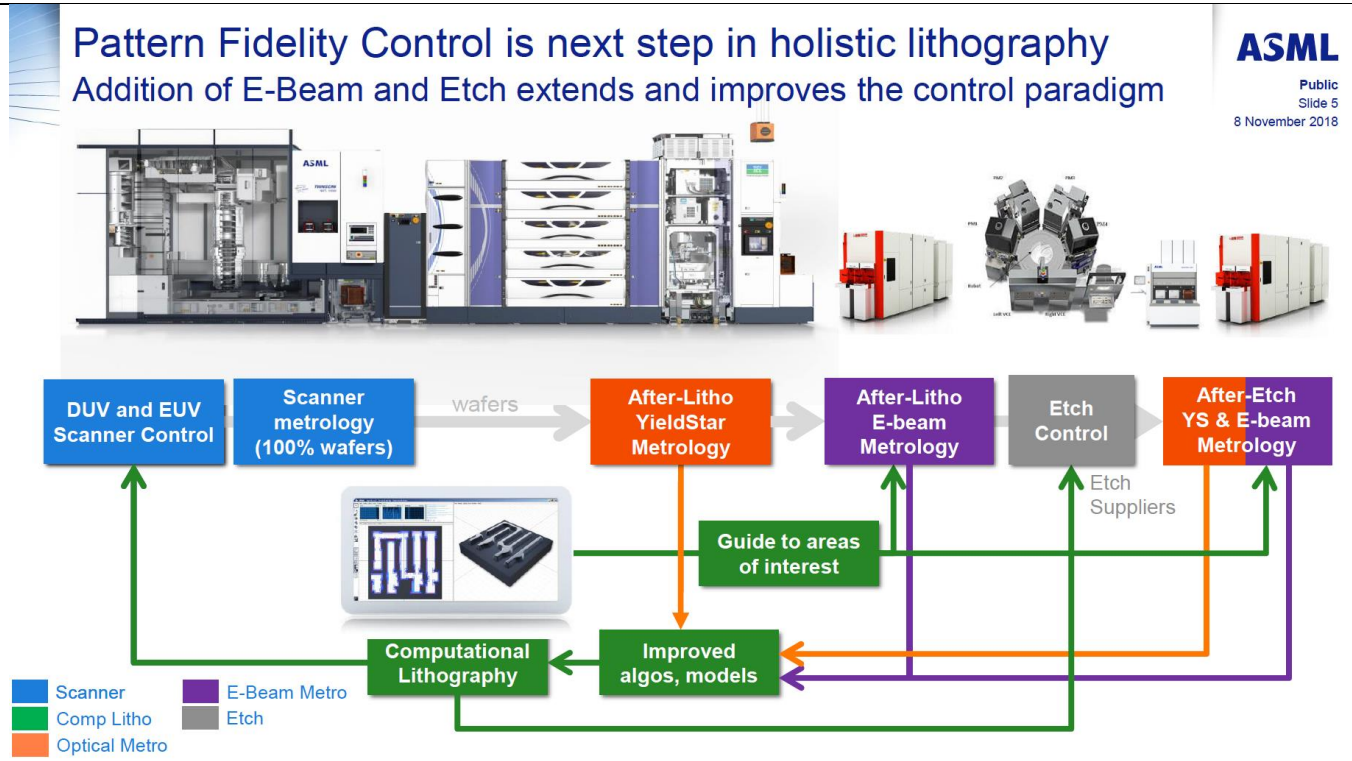
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes, as shown below:

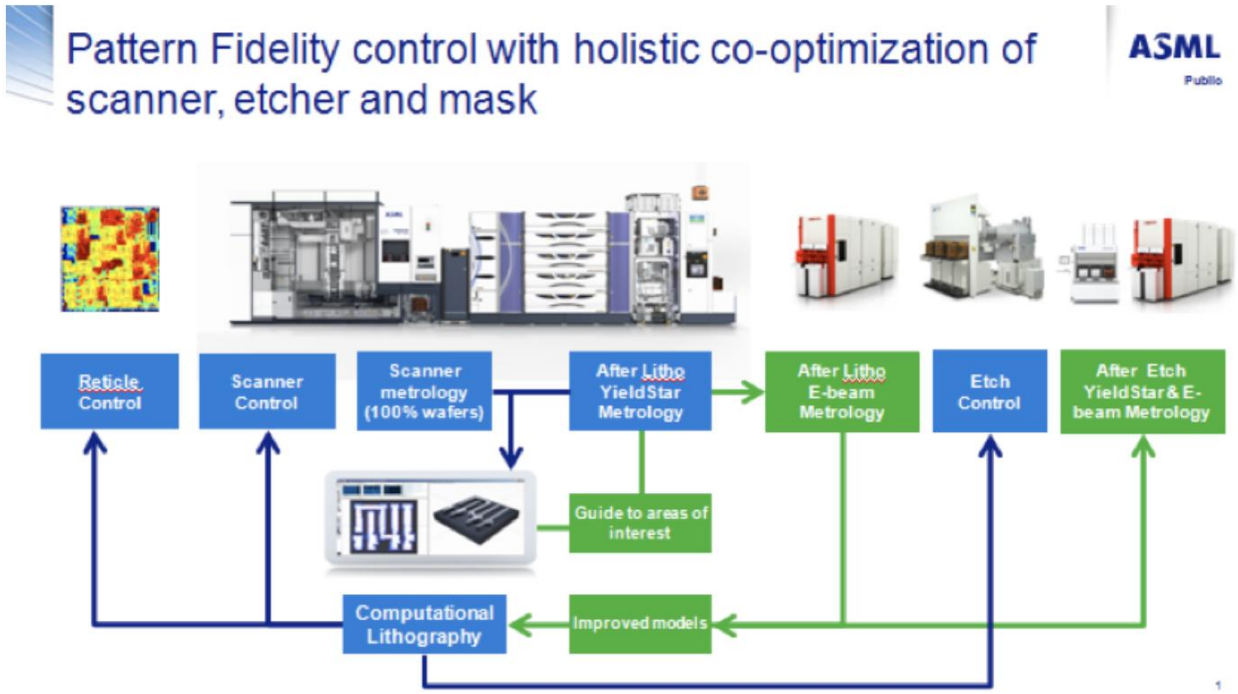
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See Applications Products and Business Opportunity at 5.

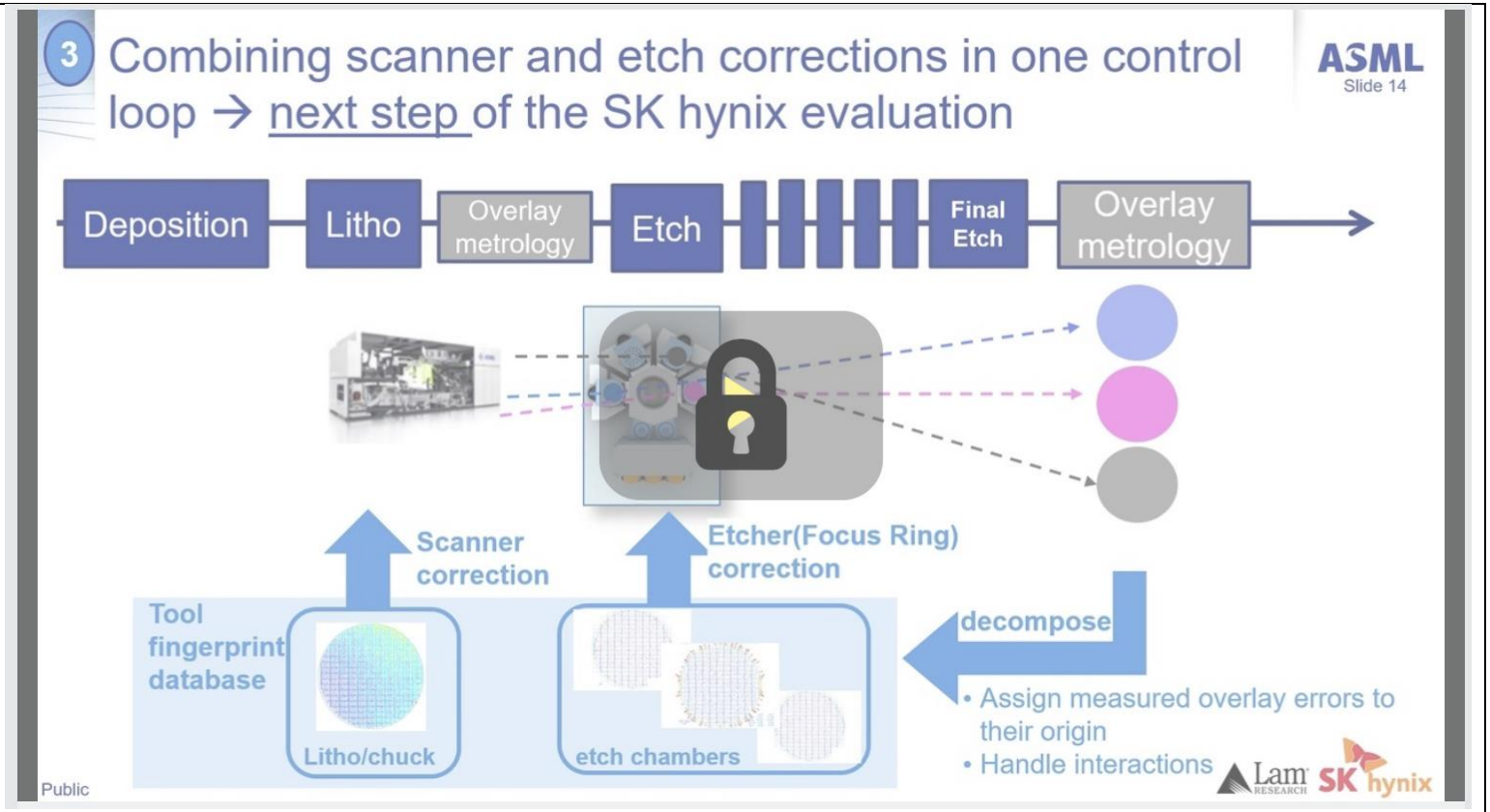
As a further example, the ’651 Infringing Instrumentalities “co-optimize[] its scanner process with etch and reticle process steps,” as shown below:



(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

See Process Complexity at 2; *see also* Scanner and Etch Optimized Corrections (showing "scanner and etch corrections in one control"):



As a further example, the'651 Infringing Instrumentalities also include a chamber for deposition of pin-on-glass, anti-reflective coating and photoresist, as shown below:

"Patterning was achieved by depositing 100nm SOC, 30nm spin-on-glass (SOG), 29nm Anti-Reflective Coating (ARC), and 105nm photoresist (PR) in an ASML Twinscan NXT:1950i 193nm immersion scanner, followed by lithographic patterning of line/space patterns."

See Atomic Layer Deposition") at 8.

34. The method of claim 31, wherein performing a process operation in a process tool on each of a	The '651 Infringing Instrumentalities perform at least one of a chemical etching process, a sputter etching process, and a reactive ion etching process in a process tool on each of a plurality of wafers. On information and belief, the '651 Infringing Instrumentalities perform at least a chemical etching process in a

plurality of wafers comprises performing at least one of a chemical etching process, a sputter etching process, and a reactive ion etching process in a process tool on each of a plurality of wafers.	process tool on each of a plurality of wafers.
35. The method of claim 31, wherein measuring a plurality of said processed wafers to determine across-wafer variations produced by said process operation comprises measuring a plurality of said processed wafers to determine across-wafer variations in a thickness of a process layer produced by said process operation.	The ’651 Infringing Instrumentalities measure a plurality of wafers to determine across-wafer variations in a thickness of a process layer produced by said process operation. For example, the ’651 Infringing Instrumentalities measure CD Uniformity, as shown below: “To provide early learning on EUV, an EUV fullfield scanner, the Alpha Demo Tool (ADT) from ASML was installed at IMEC, using a Numerical Aperture (NA) of 0.25. In this paper we report on different aspects of the ADT: the imaging and overlay performance and both short and long-term stability. For 40nm dense Lines-Spaces (LS), the ADT shows an across field overlapping process window of 270nm Depth Of Focus (DOF) at 10% Exposure Latitude (EL) and a wafer CD Uniformity (CDU) of 3nm 3σ, without any corrections for process or reticle. The wafer CDU is correlated to different factors that are known to influence the CD fingerprint from traditional lithography: slit intensity uniformity, focus plane deviation and reticle CD error.” *See* ASML EUV Alpha Demo Tool. As a further example, the ’651 Infringing Instrumentalities measure wafer overlay, as shown below: “3.1. Overlay Performance Overlay needs to follow the ITRS roadmap requirements. Relevant parameters are the stage accuracy, single machine overlay and matched machine overlay. The overlay performance of immersion systems has shown a big improvement. For the first production systems showed typical overlay of 10 nm, for the 1400i is systems overlay measurements have been done showing overlay data below 6 nm. The measured overlay data over a 9 wafer lot is

presented in Fig. 13. The data shows that today overlay performance can meet the requirements of the ITRS roadmap. For the use of the lithographic tools in a production environment, the system have to be matched to other systems, this includes the matching of a dry system to a wet system, as an example we have matched a 0.85 dry system to a 0.93 wet system."

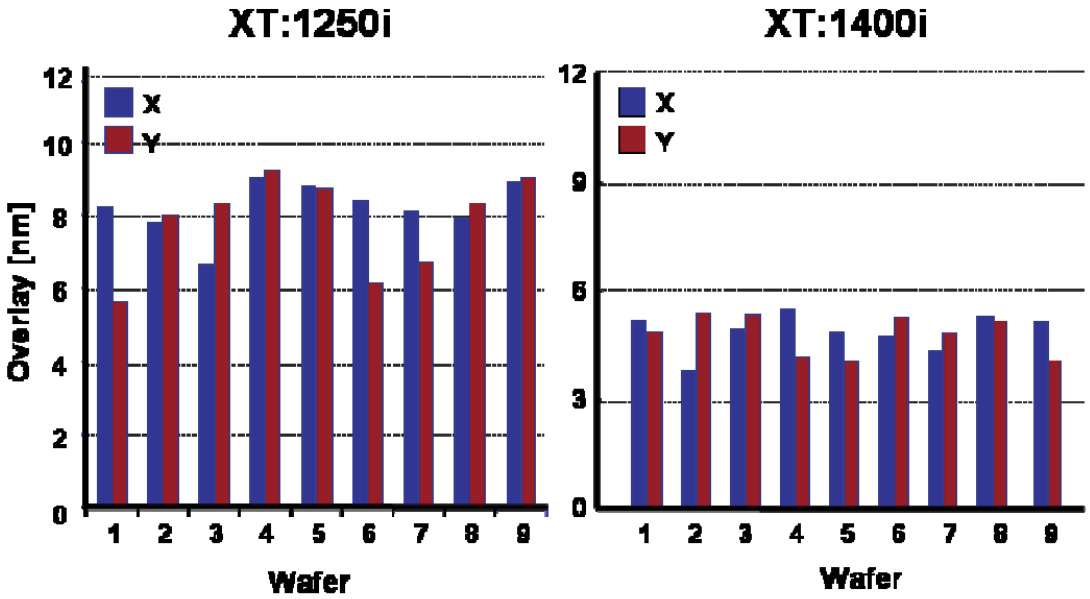


Figure 13: Overlay performance for immersion systems.

See H. Jasper et al., "Immersion lithography with an ultrahigh-NA in-line catadioptric lens and a high-transmission flexible polarization illumination," ("**Immersion Lithography with an Ultrahigh-NA In-Line Catadioptric Lens**") at 3.1, Proc. of SPIE vol. 6154 (April 2006), *available at* https://www.researchgate.net/publication/253204007_Immersion_lithography_with_an_ultrahigh-NA_in-line_catadioptric_lens_and_a_high-transmission_flexible_polarization_illumination_system/link/5efe3619458515505085d7e4/download

As a further example, the '651 Infringing Instrumentalities collect experimental overlay data obtained during operation of the TWINSCAN system, as shown below:

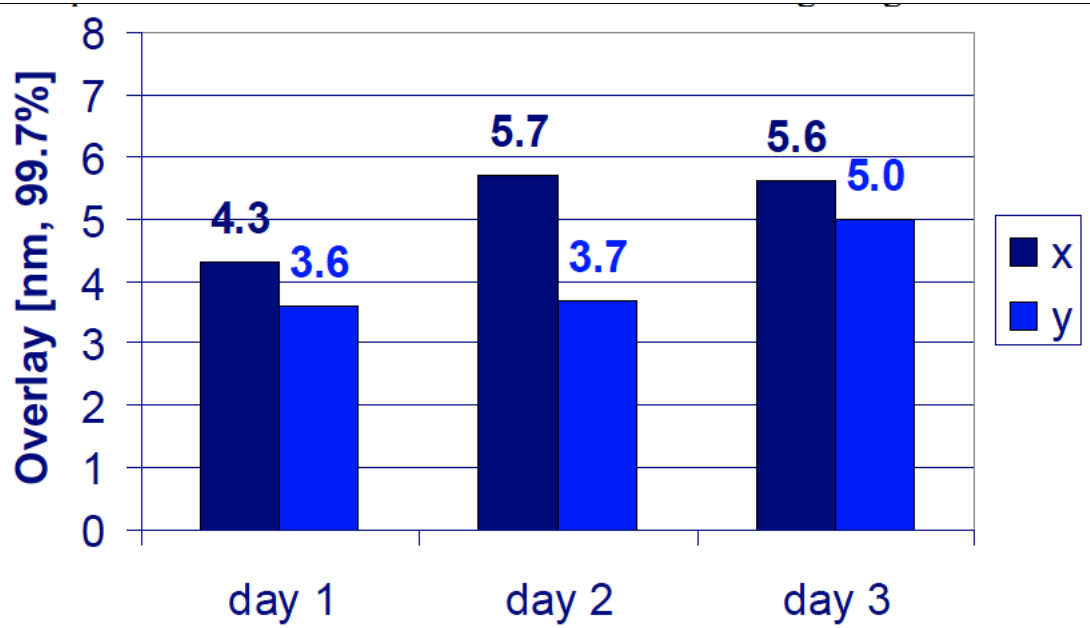
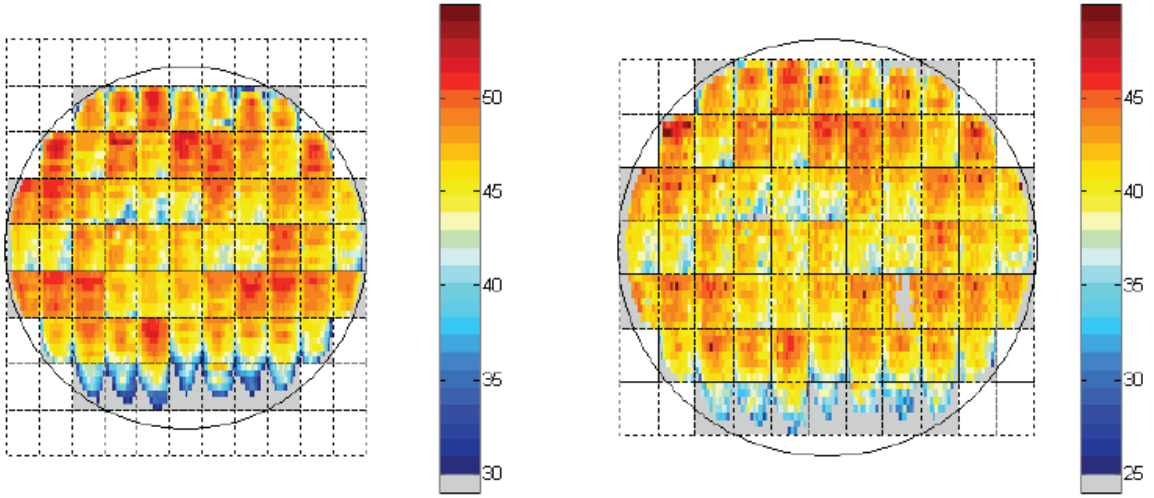


Figure 17. Single Machine Overlay (including both wafer stages).

See J. de Klerk *et al*., "Performance of a 1.35NA ArF immersion lithography system for 40nm applications," ("**ArF Immersion Lithography System**") at 11, *available at* https://work.tbadigital.com/content/flash/210/source/SPIE2007_XT1900_paper.pdf (last visited June 19, 2021).

As another example, the '651 Infringing Instrumentalities, including ASML's YieldStar system, perform measurement of wafers to determine across-wafer variations including, for example, overlay and critical dimension:

"The S-100 can handle up to 90 WpH measured with a sample plan of 3 densely measured wafers (36 CD and 36 overlay points) and 22 less-densely measured wafers (5 CD and 5 overlay points). The S-200 and T-200 can handle up to 150 WpH, which means it is roughly 67% faster. Another improvement is that most specifications are tightened."

	J. Maas et al., "YieldStar: a new metrolog platform for advanced lithography control," Proceedings of SPIE, 27th Eurpean Mask and Lithography Conference, Dresden Germany (2011), at 4; *see also id.* at Fig. 6:  *Figure 6. Wafer map data collected with YieldStar (left) and CD-SEM (right) show similar signature.* *See also* ASML, "Lithography Principles, Measuring Accuracy," *available at* https://www.asml.com/en/technology/lithography-principles/measuring-accuracy (last visited Apr. 30, 2020): "Fast, accurate wafer metrology In wafer metrology, key manufacturing parameters such as overlay (the accuracy with which two layers of a chip are aligned) and focus (how sharp the image is) are monitored by measuring how well a particular repeating pattern (the 'metrology target') is printed on the wafer. These measurements are made at marked locations across the wafer. . . . Metrology data is analyzed in control software and fed back to the lithography system in real-time, which enables customers to tune the manufacturing process further for optimal yield."
36. The method of claim 31, wherein measuring a	The '651 Infringing Instrumentalities measure a plurality of said processed wafers to determine across-wafer variations in feature sizes produced by said process operation.

plurality of said processed wafers to determine across-wafer variations produced by said process operation comprises measuring a plurality of said processed wafers to determine across-wafer variations in feature sizes produced by said process operation.	For example, the '651 Infringing Instrumentalities measure CD Uniformity, as shown below: "To provide early learning on EUV, an EUV fullfield scanner, the Alpha Demo Tool (ADT) from ASML was installed at IMEC, using a Numerical Aperture (NA) of 0.25. In this paper we report on different aspects of the ADT: the imaging and overlay performance and both short and long-term stability. For 40nm dense Lines-Spaces (LS), the ADT shows an across field overlapping process window of 270nm Depth Of Focus (DOF) at 10% Exposure Latitude (EL) and a wafer CD Uniformity (CDU) of 3nm 3σ, without any corrections for process or reticle. The wafer CDU is correlated to different factors that are known to influence the CD fingerprint from traditional lithography: slit intensity uniformity, focus plane deviation and reticle CD error." *See* J.V. Hermans et al., "Stability and imaging of the ASML EUV Alpha Demo Tool" ("ASML EUV Alpha Demo Tool"), Proc. of SPIE vol. 7271 at Abstract, *available at* https://www.researchgate.net/profile/Anne-Marie-Goethals/publication/253055399_Stability_and_imaging_of_the_ASML_EUV_alpha_demo_tool/links/5492e4090cf209fc7e9f8486/Stability-and-imaging-of-the-ASML-EUV-alpha-demo-tool.pdf (last visited June 19, 2021) As a further example, the '651 Infringing Instrumentalities determine across-wafer variations in feature sizes via overlay and CD data, as shown below: "3.1. Overlay Performance Overlay needs to follow the ITRS roadmap requirements. Relevant parameters are the stage accuracy, single machine overlay and matched machine overlay. The overlay performance of immersion systems has shown a big improvement. For the first production systems showed typical overlay of 10 nm, for the 1400i is systems overlay measurements have been done showing overlay data below 6 nm. The measured overlay data over a 9 wafer lot is presented in Fig. 13. The data shows that today overlay performance can meet the requirements of the ITRS roadmap. For the use of the lithographic tools in a production environment, the system have to be matched to other systems, this includes the matching of a dry system to a wet system, as an example we have matched a 0.85 dry system to a 0.93 wet system."

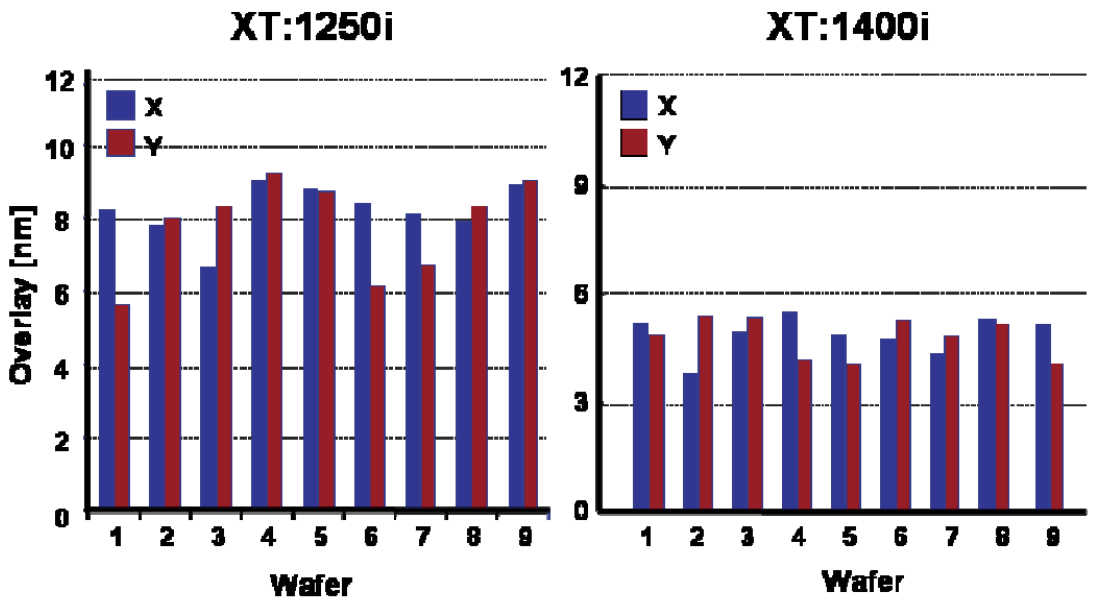


Figure 13: Overlay performance for immersion systems.

See Immersion Lithography with an Ultrahigh-NA In-Line Catadioptric Lens at 3.1.

As a further example, the ’651 Infringing Instrumentalities collect experimental overlay data obtained during operation of the TWINSCAN system to determine across-wafer variations in feature sizes, as shown below:

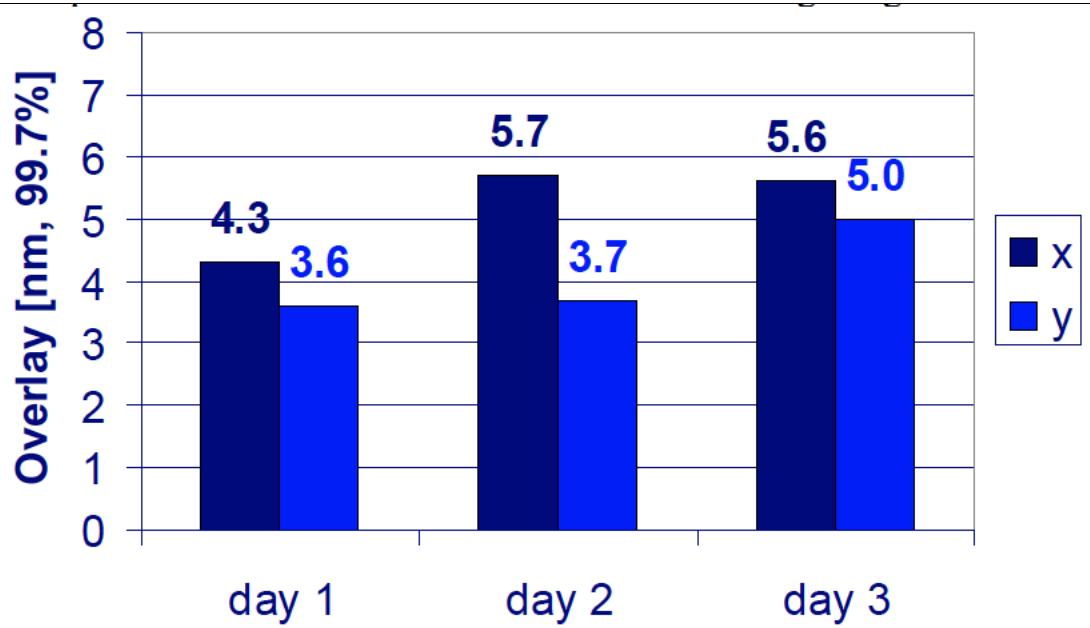


Figure 17. Single Machine Overlay (including both wafer stages).

See ArF Immersion Lithography System at 11.

As another example, the '651 Infringing Instrumentalities, including ASML's YieldStar system, perform measurement of wafers to determine across-wafer variations in feature sizes including, for example, overlay and critical dimension:

"The S-100 can handle up to 90 WpH measured with a sample plan of 3 densely measured wafers (36 CD and 36 overlay points) and 22 less-densely measured wafers (5 CD and 5 overlay points). The S-200 and T-200 can handle up to 150 WpH, which means it is roughly 67% faster. Another improvement is that most specifications are tightened."

J. Maas et al., "YieldStar: a new metrolog platform for advanced lithography control," Proceedings of SPIE, 27th Eurpean Mask and Lithography Conference, Dresden Germany (2011), at 4; *see also id.* at Fig. 6:

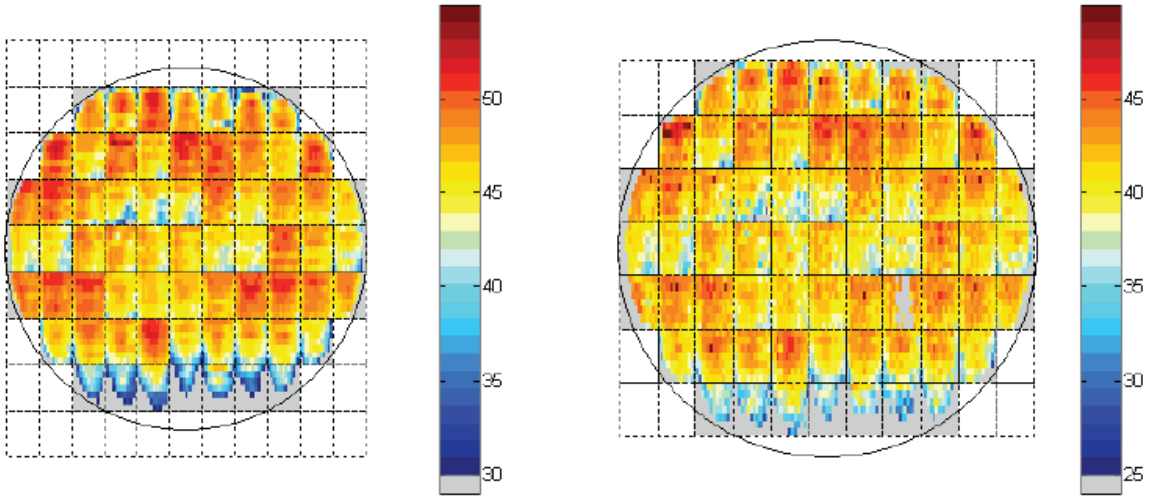


Figure 6. Wafer map data collected with YieldStar (left) and CD-SEM (right) show similar signature.

See also ASML, "Lithography Principles, Measuring Accuracy," *available at* https://www.asml.com/en/technology/lithography-principles/measuring-accuracy (last visited Apr. 30, 2020):

"Fast, accurate wafer metrology In wafer metrology, key manufacturing parameters such as overlay (the accuracy with which two layers of a chip are aligned) and focus (how sharp the image is) are monitored by measuring how well a particular repeating pattern (the 'metrology target') is printed on the wafer. These measurements are made at marked locations across the wafer. . . . Metrology data is analyzed in control software and fed back to the lithography system in real-time, which enables customers to tune the manufacturing process further for optimal yield."

37. The method of claim 31, wherein adjusting, based upon said measured across-wafer variations, a plane of a	The '651 Infringing Instrumentalities perform at least one of raising, lowering and tilting, based upon said measured across-wafer variations, said plane of said surface of said adjustable wafer stage. For example, the TWINSCAN system adjusts the surface of the wafer stage by wafer leveling based on the measured across-wafer variations (e.g., using metrology) via vertical actuators to a second plane that is offset from

surface of an adjustable wafer stage comprises performing at least one of raising, lowering and tilting, based upon said measured across-wafer variations, said plane of said surface of said adjustable wafer stage.	and approximately parallel to said first plane (e.g., in the "z direction"): "Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively." *See* Position Control at 41; *see also id.* at 38 ("For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metro-frame world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor."). As another example, the TWINSCAN system includes a linear motor to drive the wafer stage in the x direction while simultaneously acting as a guiding beam for a roller bearing. The x motor itself is moved in the y direction as well as in the rotational direction θ around the z axis: "One linear motor drives the stage in the x direction, while simultaneously acting as a guiding beam for a roller bearing. The x motor itself can be moved in the y direction as well as in a rotational direction u around the z axis, by means of two linear y motors. These motors also act as a guiding beam for the bearings of the x-motor stators." *See* Position Control at 31. Also, the wafer stage's stage coordinates for raising the wafer stage are defined by X, Y, and Z coordinates: "The next step is then the conversion of forces in the stage coordinate system into forces $f^{T}m$ = (Fx1 Fy1 Fy2 Fz1 Fz2 Fz3) for the individual motors. This step, which is called gain balancing, is completely determined by the geometric actuator layout." *See* Position Control at 41. As an example, the vertical directions (or raising) of the wafer stage (e.g., from a first plane to a second plane) can be achieved using Lorentz actuators: "To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result"

	See Position Control at 40. As a further example, the TWINSCAN wafer stage has a surface that can be lowered using vertical actuators (e.g., in the "z direction"): "Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively." *See* Position Control at 41; *see also id.* at 38 ("For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metroframe world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor."). As an example, the TWINSCAN system includes a linear motor to drive the wafer stage in the x direction while simultaneously acting as a guiding beam for a roller bearing. The x motor itself is moved in the y direction as well as in the rotational direction θ around the z axis: "One linear motor drives the stage in the x direction, while simultaneously acting as a guiding beam for a roller bearing. The x motor itself can be moved in the y direction as well as in a rotational direction u around the z axis, by means of two linear y motors. These motors also act as a guiding beam for the bearings of the x-motor stators." *See* Position Control at 31. Also, the wafer stage's stage coordinates for lowering are defined by X, Y, and Z coordinates: "The next step is then the conversion of forces in the stage coordinate system into forces $f^{T}m$ = (Fx1 Fy1 Fy2 Fz1 Fz2 Fz3) for the individual motors. This step, which is called gain balancing, is completely determined by the geometric actuator layout." *See* Position Control at 41. As an example, the vertical directions (e.g., lowering) of the wafer stage can be achieved using Lorentz actuators:

"To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result"

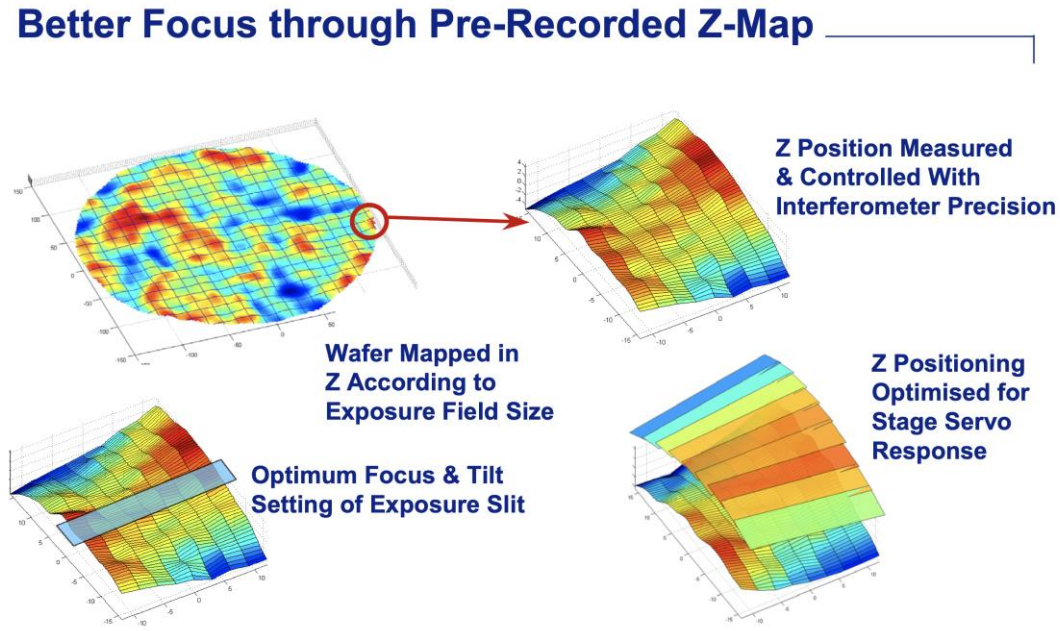
See Position Control at 40.

As a further example, the wafer stage in TWINSCAN can be tilted, as shown below:

"The reason for this lies in the scanning levelling: when the stage has to tilt around a horizontal axis to keep the wafer in focus, the stage tends to rotate around its center of mass, introducing a horizontal shift on wafer level."

See Perspective on Stage Dynamics and Control at 2.

As a further example, TWINSCAN uses "optimum tilt" to achieve "better focus," as shown below:



See "TWINSCAN AT:1100 Imaging to Enable the Next Generation of Chips 100nm volume manufacturing on 300mm wafers" at 19.

As a further example, in TWINSCAN, non-correctable errors in wafer surface topography can be remedied by

	adjusting stage tilt, as shown below: We define the wafer non-correctable focus errors, NCE, as the wafer surface topography that cannot be completely compensated due to the finite size of the exposure slit. For a static exposure, these non-correctable errors correspond directly to defocus errors. However, during a scanned exposure, the non-correctable errors change continuously as the slit is scanned over a particular position on the wafer. In the latter case, the average value of the non-correctable errors over the exposure time defines the average defocus that this position experiences during the exposure. We define this value that depends on the slit size and on the spatial-frequency and amplitude of the wafer topography as simulated defocus, or as the Moving Average in the z-direction (MA(z)). Changes in the topography that are larger then the slit dimensions can be leveled by adjusting the stage height and tilt angle accordingly. If the topography variation occurs over distances that are smaller than the slit dimensions, the height changes cannot be leveled effectively. *See* B. Lafontaine *et al*., "Study of the influence of substrate topography on the focusing performance of advanced lithography scanners" ("**Influence of Substrate Topography**") (Feb. 27, 2003), *available at* https://www.researchgate.net/publication/228428889_Study_of_the_influence_of_substrate_topography_on_the_focusing_performance_of_advanced_lithography_scanners (last visited June 19, 2021).
72. A method, comprising: providing a process chamber comprised of a wafer stage, said wafer stage having a surface that is adjustable and located in a first plane;	The '651 Infringing Instrumentalities provide a process chamber comprised of a wafer stage, the wafer stage having a surface that is adjustable and located in a first plane. For example, each TWINSCAN system includes a process chamber. *See* ASML Corproate Responsibility Report 2015, *available at* https://www.sec.gov/Archives/edgar/data/937966/000093796616000015/corporateresponsibiltyrepo.htm; *see also* ASML products, *available at* https://www.asml.com/en/products/duv-lithography-systems:

TWINSCAN NXT:2000i

The TWINSCAN NXT:2000i is our state-of-the-art immersion lithography system currently being ramped in high-volume manufacturing of the 7 nm Logic and advanced DRAM nodes

TWINSCAN NXT:1980Di

Introduced in 2015, the TWINSCAN NXT:1980Di delivers high productivity with high reliability: system uptime is at > 97% worldwide.

TWINSCAN NXT:1970Ci

The TWINSCAN NXT:1970Ci delivers high productivity and excellent image resolution using a dual-stage concept.

TWINSCAN NXT:1965Ci

The TWINSCAN NXT:1965Ci delivers high productivity and excellent image resolution using a dual-stage concept.

TWINSCAN XT:1460K

The TWINSCAN XT:1460K is our latest-generation dual-stage 'dry' lithography system, offering excellent overlay and imaging performance at high productivity.

TWINSCAN XT:1060K

The TWINSCAN XT:1060K is ASML's most advanced KrF (krypton fluoride) laser 'dry' lithography system.

TWINSCAN XT:860M

The TWINSCAN XT:860M is designed using state-of-the-art optics for volume 300 mm wafer production at and below 110 nm resolution.

TWINSCAN XT:400L

The TWINSCAN XT:400L is ASML's latest-generation i-line lithography system, using a mercury vapor lamp to print features down to 220 nm.

TWINSCAN XT:1460K

The TWINSCAN XT:1460K is our latest-generation dual-stage 'dry' lithography system, offering excellent overlay and imaging performance at high productivity.

TWINSCAN XT:1060K

The TWINSCAN XT:1060K is ASML's most advanced KrF (krypton fluoride) laser 'dry' lithography system.

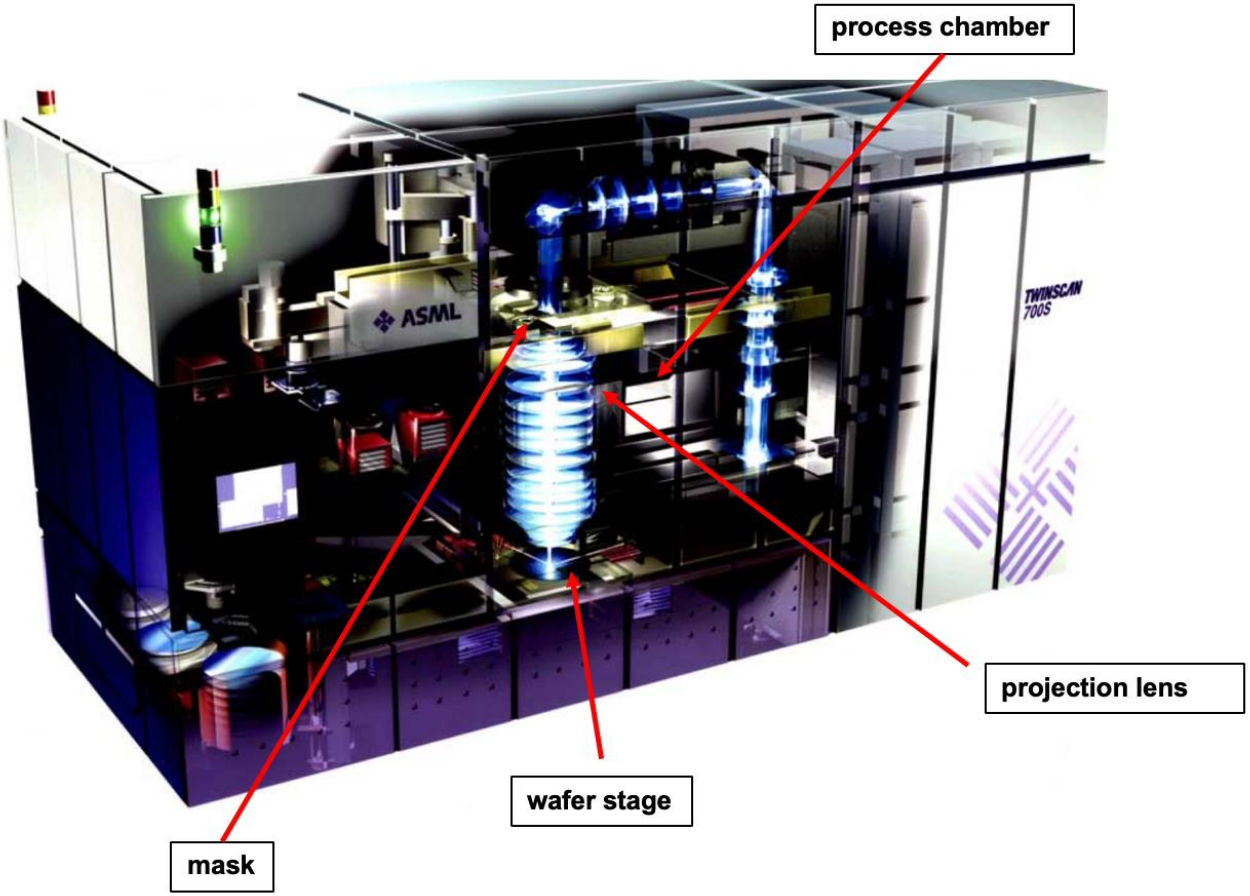
TWINSCAN XT:860M

The TWINSCAN XT:860M is designed using state-of-the-art optics for volume 300 mm wafer production at and below 110 nm resolution.

TWINSCAN XT:400L

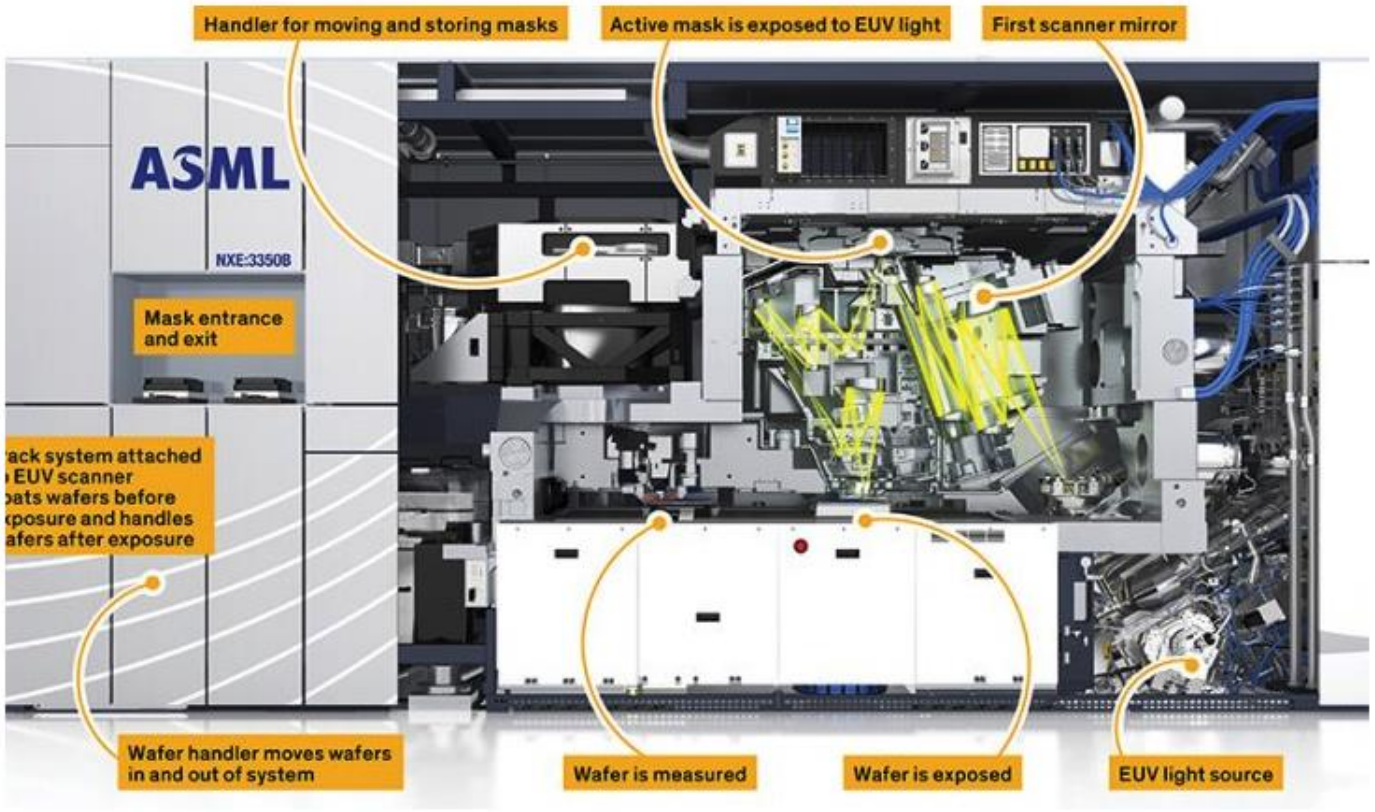
The TWINSCAN XT:400L is ASML's latest-generation i-line lithography system, using a mercury vapor lamp to print features down to 220 nm.

As an example, each TWINSCAN system includes a process chamber as shown below:



See ASML Twinscan Technical Backgrounder, *available at* https://www.chiphistory.org/landmarks/lm_asml_twinscan_step_and_scan_aligner_1990/ip_asml_twinscan_step_and_scan_aligner_1990.htm (annotated).

See also EUV Lithography tools shipping in 2018, available at https://www.nextbigfuture.com/2017/04/euv-lithography-tools-shipping-in-2018.html:



TSMC uses, for example, ASML's extreme ultraviolet (EUV) lithography systems on 5nm and 7nm products. *See e.g.*, TSMC 5nm Technology, *available at* https://www.tsmc.com/english/dedicatedFoundry/technology/5nm.htm ("TSMC's 5nm Fin Field-Effect Transistor (FinFET) process technology is optimized for both mobile and high performance computing applications. It is scheduled to start risk production in the second half of 2019. TSMC's 5nm technology is the second available EUV process technology. It showed promising imaging capability with expected good wafer yield."); *see also TSMC Celebrates 25th Anniversary of the North American Technology Symposium, available at* https://www.tsmc.com/tsmcdotcom/PRListingNewsAction.do?action=detail&language=E&newsid=THGOWQTHTH ("The World's first commercially available 7nm EUV in volume production in 2019").

As another example, the TWINSCAN system performs the method of providing a process chamber:

See ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30 2019).

As a further example, the TWINSCAN system provides a process chamber comprised of a wafer stage, said wafer stage having a surface that is adjustable and located in a first plane:

See ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30 2019).

The process chamber can be used for wafer exposure during lithography:

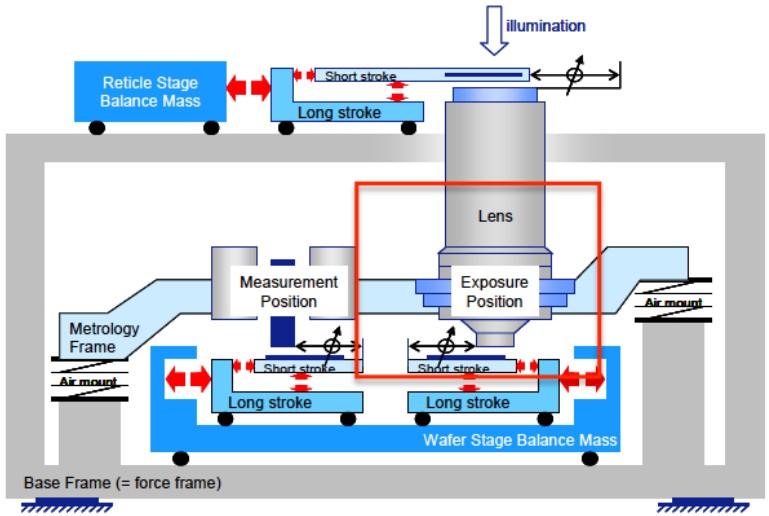


Figure 5. TWINSCAN™ dynamic architecture

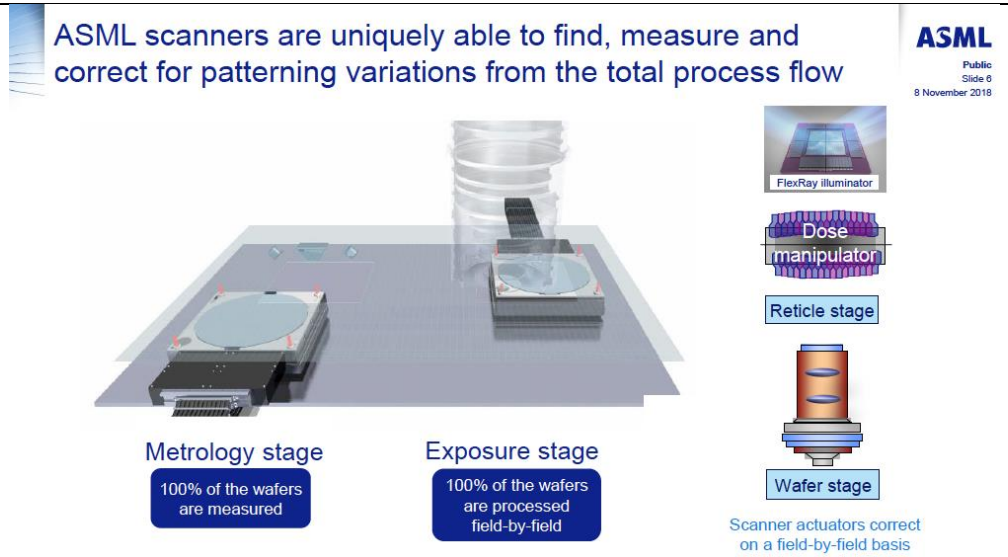
See Perspective on Stage Dynamics and Control at 3.

The process chamber includes an adjustable wafer stage having a surface that is adjustable and located in a first plane:

"In Figure 4, the table holding the wafer is called the mirror block because of the mirroring side surfaces, which allow interferometric position measurement (IFM)."

See Position Control at 31.

For example, the adjustable wafer stage or mirror block (whose surface is located in a first plane) of the TWINSCAN system is shown below:

	 *See* Applications Products and Business Opportunity at 6.
adjusting said surface of said wafer stage by raising said surface of said wafer stage to a position wherein said surface of said wafer stage is positioned in a second plane that is offset from and approximately parallel to said first plane;	The ’651 Infringing Instrumentalities adjust the surface of the wafer stage by raising said surface of said wafer stage to a position wherein said surface of said wafer stage is positioned in a second plane that is offset from and approximately parallel to said first plane. For example, the TWINSCAN system adjusts the surface of the wafer stage by raising the wafer stage via wafer leveling using vertical actuators to a second plane that is offset from and approximately parallel to said first plane (e.g., in the “z direction”): “Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively.” *See* Position Control at 41; *see also id.* at 38 (“For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metro-frame world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor.”). As another example, the TWINSCAN system includes a linear motor to drive the wafer stage in the x direction

	while simultaneously acting as a guiding beam for a roller bearing. The x motor itself is moved in the y direction as well as in the rotational direction θ around the z axis such that the surface of the wafer stage is positioned in a second plane that is offset from and approximately parallel to said first plane: "One linear motor drives the stage in the x direction, while simultaneously acting as a guiding beam for a roller bearing. The x motor itself can be moved in the y direction as well as in a rotational direction u around the z axis, by means of two linear y motors. These motors also act as a guiding beam for the bearings of the x-motor stators." *See* Position Control at 31. Also, the wafer stage's stage coordinates for raising the wafer stage are defined by X, Y, and Z coordinates: "The next step is then the conversion of forces in the stage coordinate system into forces $f^{T}m$ = (Fx1 Fy1 Fy2 Fz1 Fz2 Fz3) for the individual motors. This step, which is called gain balancing, is completely determined by the geometric actuator layout." *See* Position Control at 41. As an example, the vertical directions (or raising) of the wafer stage (e.g., from a first plane to a second plane) can be achieved using Lorentz actuators: "To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result" *See* Position Control at 40. A diagram showing the vertical connection that facilitates the vertical movement (or raising) of the wafer stage is shown below:

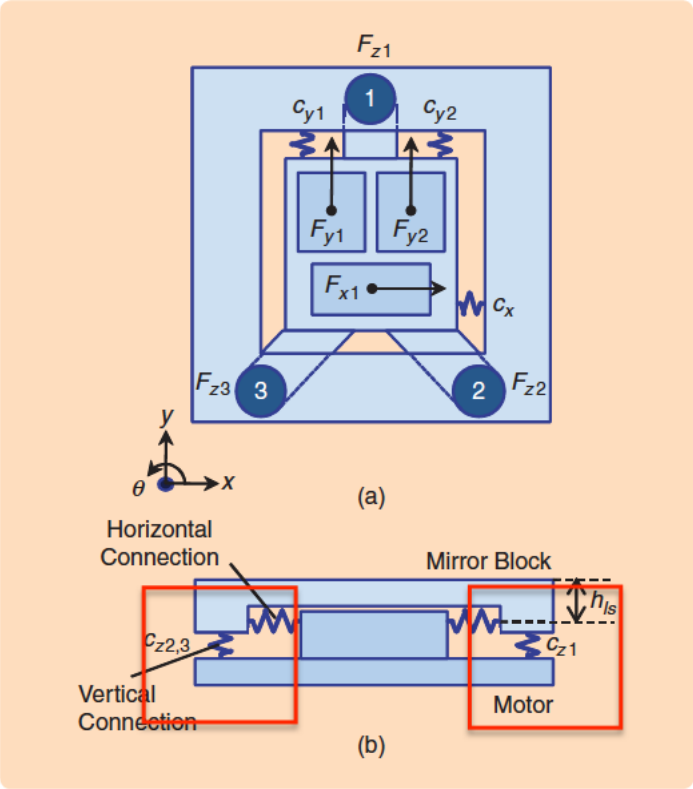


FIGURE 26 Stage layout with motor connection stiffness. The motor

See Position Control at 41 (annotated).

In one example, the wafer stage rotates around the center of the lens above it in the vertical directions:

"The stage now rotates around the lens center instead of its center of mass. Especially in the vertical directions, the applicable rotations may show a high acceleration, depending on the vertical topology of the wafer surface."

See Position Control at 42.

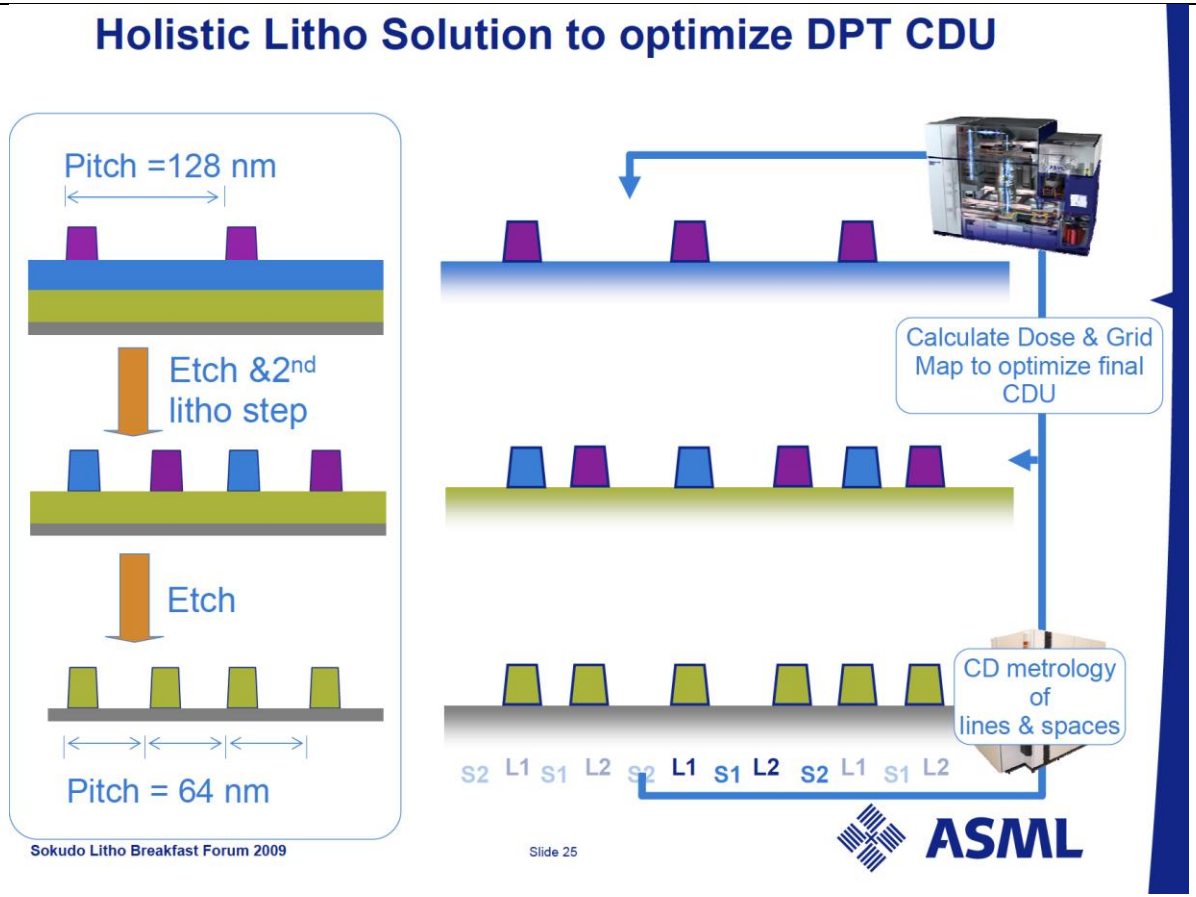
Also, the TWINSCAN system adjusts the surface of the wafer stage such that the surface of the wafer stage is positioned in a second plane that is offset from and approximately parallel to the first plane:

"After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the

	step motion indicate the usability of the system for imaging." *See* Position Control at 35. As another example, the TWINSCAN system adjusts the surface of the wafer stage such that the surface of the wafer stage is positioned in a second plane that is offset from and approximately parallel to the first plane by making such an adjustment at the time when the surface is mapped in horizontal and vertical planes: "At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40.
positioning a wafer on said wafer stage; and	The '651 Infringing Instrumentalities position a wafer on the wafer stage. For example, the TWINSCAN system positions the wafer on the wafer stage: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35. The wafer is also positioned onto the wafer stage so that exposure can start: "At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40.
performing a process operation on said wafer	The '651 Infringing Instrumentalities perform a process operation on the wafer position on the wafer stage.

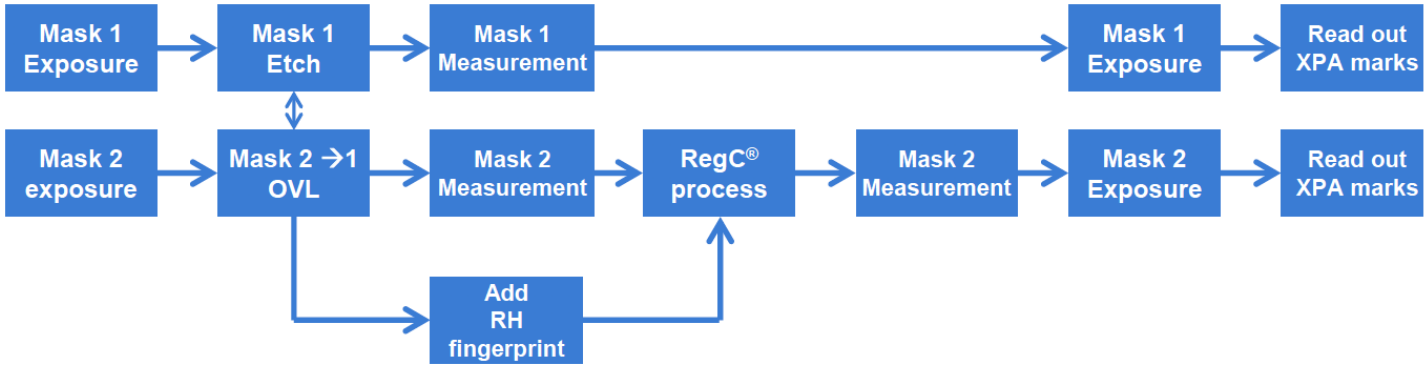
positioned on said wafer stage.	For example, the TWINSCAN system performs stepper imaging or double patterning as part of the step-and-scan in exposing a wafer: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35. Once the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself, the stage positioned under the projection lens is aligned to the reticle by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start: "Stage position measurement is now performed in all degrees of freedom by interferometers, with reference beams directed at the projection lens. This method provides a direct relative measurement of the position with respect to the lens. At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40. As another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage, as shown below: "A solution was found by equipping the system with two wafer stages [7]. While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. The increased stage acceleration and speed further improves throughput." *See* Position Control at 39-40; *see also id*. at 37:

	"Figure 16 shows a more detailed timing diagram of the stage movement during a scan. Figure 16(b) shows an acceleration setpoint profile, which in this example is a thirdorder profile instead of the previously used second-order profile. Figure 16(a) shows the velocity setpoint profile. At t5t0, the acceleration phase ends, and a constant velocity is reached. After a certain settling time, which allows the remaining controller error to be reduced to an acceptable value, the first point in the die to be exposed enters the illumination slit at t5t1. At t5t2, this first point on the die leaves the slit again. The stage-positioning errors in the interval 3t1, t2 4 determine the effect on overlay and imaging. Hence, the calculated MA and MSD values over this first interval correspond to the effect of positioning errors on the first point in the die. At t5t3, the last point of the die enters the slit, and, finally, at t5t4 the die leaves the slit again, making the interval 3t3, t4 4 the last window over which MA and MSD values need to be calculated. Hence, the total scan length of the stage equals the length of the die, plus the height of the slit, plus the length needed for settling of the stage. After t5t4, the stage decelerates again to standstill or follows another trajectory that brings the stage to the start of the next die." As a further example, "the ASML® TWINSCAN® NXE:3350B production-ready EVU system produces 125 computer wafers per hour using 13.5 nm wavelength light." *See* V. Marra, "ASML Advances Computing Breakthroughs with Multiphysics Modeling" at 4. As yet another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage:



See Holistic View of Lithography at 25.

As a further example, the '651 Infringing Instrumentalities, including the TWINSCAN system, perform "Mask 1 Etch":



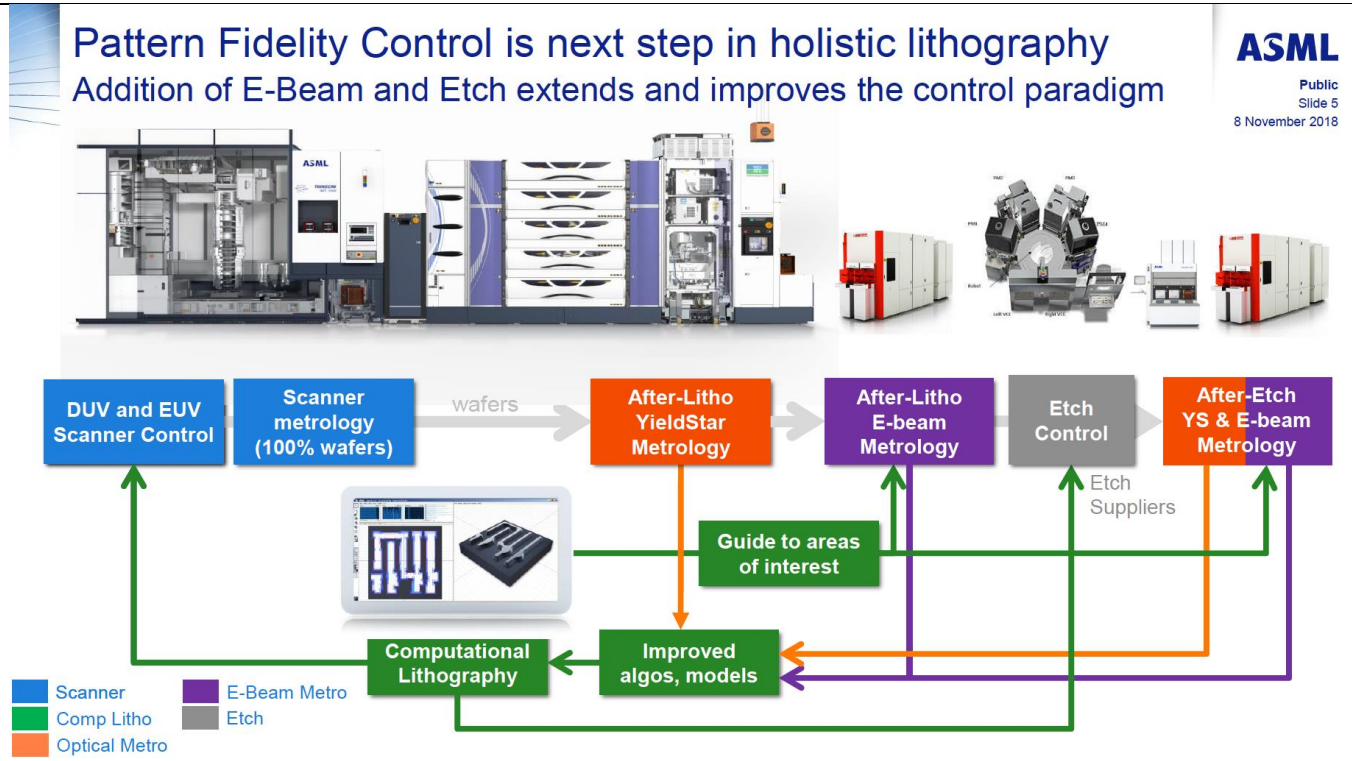
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM Corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes:

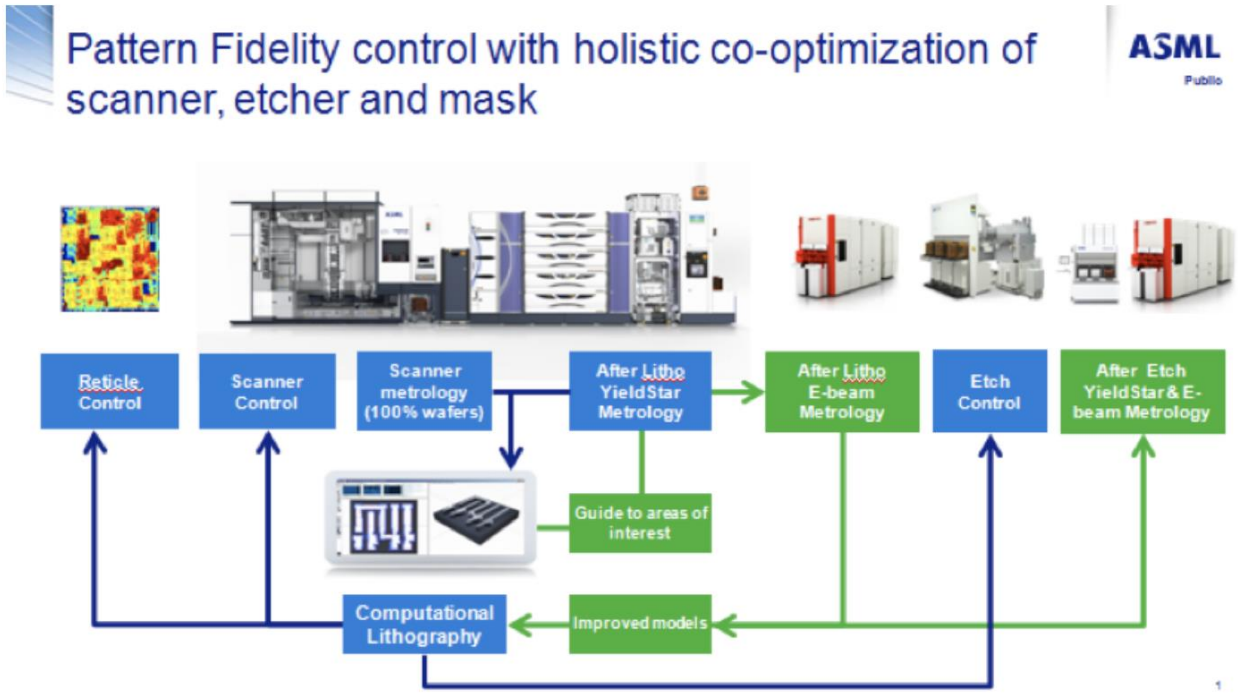
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

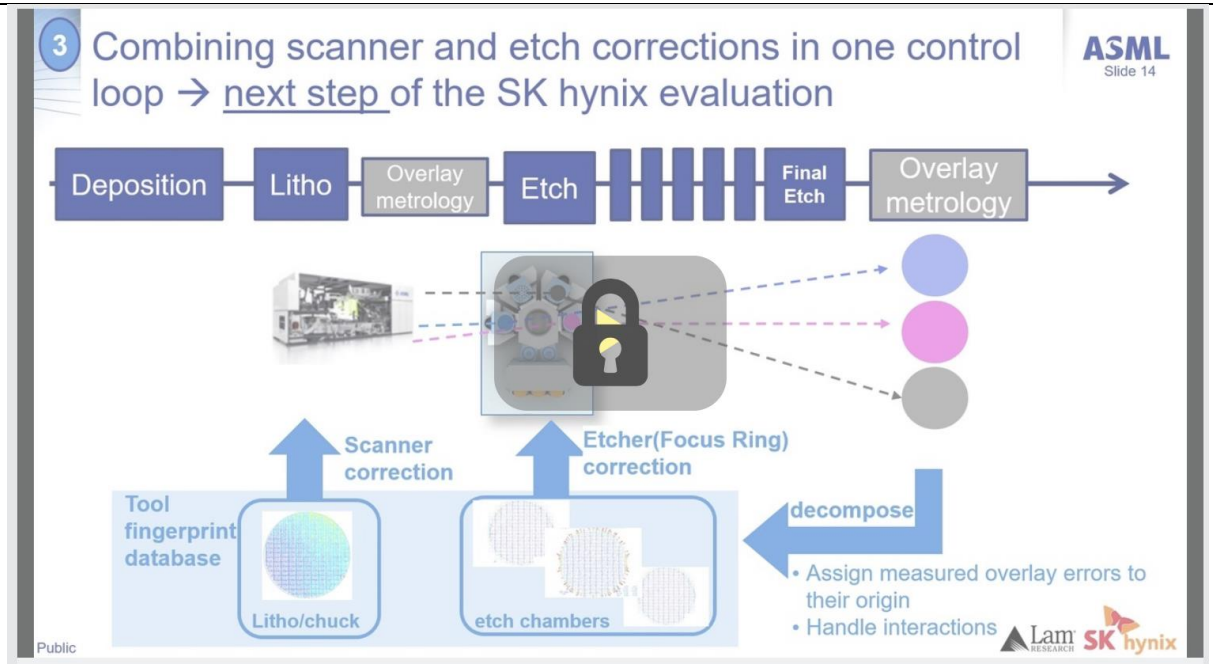
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:

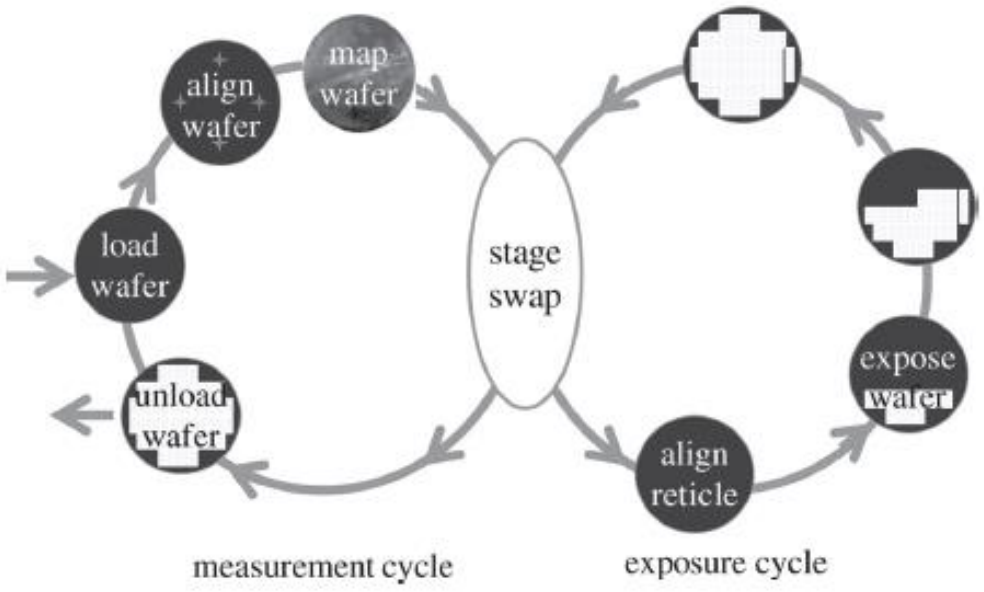


(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

See Process Complexity at 2; *see also* Scanner and Etch Co-optimized Corrections (showing "combining scanner and etch corrections in one control"):

	
73. The method of claim 72, wherein positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage after said wafer stage has been adjusted.	The ’651 Infringing Instrumentalities position a wafer on the wafer stage after the wafer stage has been adjusted. For example, the TWINSCAN system positions the wafer on the exposure table of the dual-wafer stage after the exposure of a previous wafer is done and the exposure table is adjusted to receive a new wafer for the next cycle of exposure. *See, e.g.,* Stage Positioning Management at 1-2: “These systems are designed as wafer scanners which Performance prediction for Stage Positioning Measurement (SPM) 1 CHAPTER 1. INTRODUCTION perform the exposure process in step and scan fashion as presented in Figure 1.1. The reticle with circuit pattern is placed on a reticle stage (RS), whereas the silicon wafer is placed on a wafer stage (WS). During the scan movement the light is switched on with a desired dose and the exposure process starts. The stages move according to each other performing synchronized zig-zag movements. Next during the step movement the light is switched o , the reticle goes back to its initial position and the silicon wafer is prepared for exposure of a next die. The process repeats itself until all of the dies have been processed. Next, the reticle mask is replaced with a new one and the process can start all over again, exposing a new layer on top of the previous one. The exposure of consecutive layers needs to be done with nanometer precision in order to deliver highest quality circuits.”

74. The method of claim 72, wherein positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage before said wafer stage is adjusted.	The ’651 Infringing Instrumentalities position a wafer on the wafer stage after the wafer stage has been adjusted. For example, the TWINSCAN system positions the wafer on the measurement table of the dual-wafer stage before the stage position of the measurement table is adjusted: “While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. T.” *See* Position Control at 35. *See also* Stage Positioning Management at 3:  Figure 1.3: The process steps in TWINSCAN machine [18]

75. The method of claim 72, wherein adjusting said surface of said wafer stage comprises adjusting said surface of said wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage.	The ’651 Infringing Instrumentalities adjust the surface of the wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage. For example, the TWINSCAN system actuates six Lorentz actuators that are mounted between the air foot and the wafer stage: “Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively.” *See* Position Control at 41. Generally, the wafer stage is equipped with DOF Lorentz actuators (e.g., three DOF actuators for the horizontal directions and three DOF actuators for the vertical directions): “The table also had vertical movement directions for the purpose of focusing the wafer in the image plane of the lens, requiring a measurement of the distance of the wafer to the lens by means of a level sensor system. The horizontal stage position was measured by an interferometer system. The stage was guided by means of mechanical bearings ‘rolling’ over the motor beams. With regard to controlling the stage, the horizontal controllers (3-DOF) acted independently from the vertical directions (also 3-DOF).” *See* Perspective on Stage Dynamics and Control at 1. As an example, for the x and y direction, the wafer table is adjusted by three Lorentz actuators such that the stage floats over a granite stone by means of an air bearing and the Lorentz actuators are connected to this granite stone:

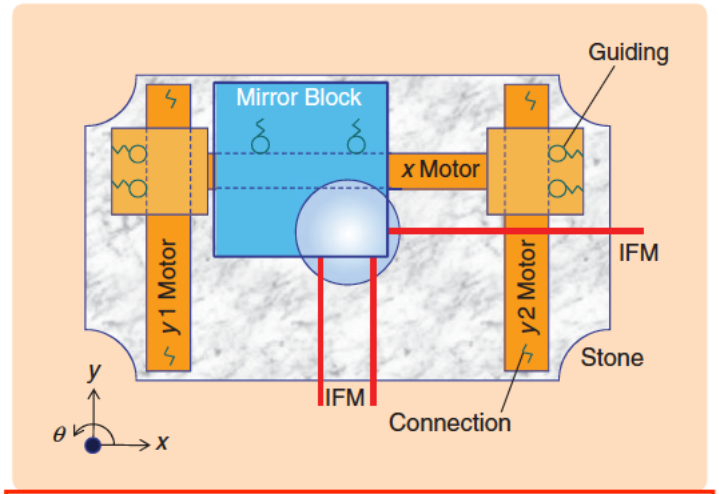


FIGURE 5 Wafer stage top view. The wafer table is driven by three actuators, two of which drive the stage in the *y* direction and the remaining one in the *x* direction. The linear actuators also function as a guide for the horizontal motion, cooperating with ball bearings in the mover. The stage floats over a granite stone by means of an air bearing, and the linear actuators are connected to this stone as well. Interferometers measure the stage position, making use of mirroring side surfaces of the stage.

See Position Control at 31 (annotated).

In total, the TWINSCAN includes 6-DOF Lorentz actuators and 6-DOF stage control, in addition to offline leveling:

"In TWINSCAN™, a further perfection in the basic design was made by using balance masses, full 6-DOF Lorentz actuators and 6-DOF stage control, in addition to off-line levelling."

See Perspective on Stage Dynamics and Control at 3.

77. A method, comprising: providing a process chamber comprised of a wafer stage, said wafer stage	The '651 Infringing Instrumentalities provide a process chamber comprised of a wafer stage, the wafer stage having a surface that is adjustable and located in a first plane. For example, each TWINSCAN system includes a process chamber. *See* ASML Corproate Responsibility Report 2015, *available at*

having a surface that is adjustable and located in a first plane;	https://www.sec.gov/Archives/edgar/data/937966/000093796616000015/corporateresponsibiltyrepo.htm; *see also* ASML products, *available at* https://www.asml.com/en/products/duv-lithography-systems:

TWINSCAN XT:1460K

The TWINSCAN XT:1460K is our latest-generation dual-stage 'dry' lithography system, offering excellent overlay and imaging performance at high productivity.

TWINSCAN XT:1060K

The TWINSCAN XT:1060K is ASML's most advanced KrF (krypton fluoride) laser 'dry' lithography system.

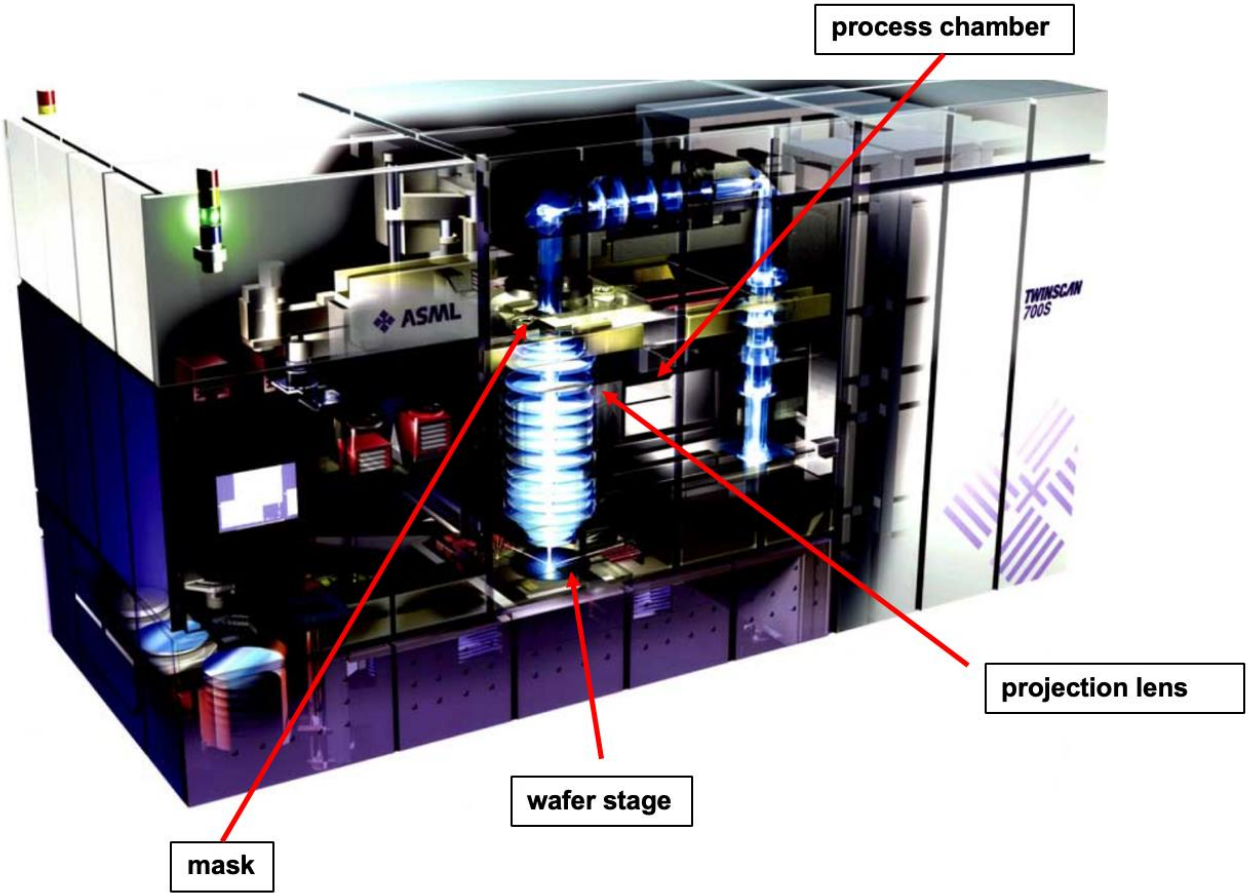
TWINSCAN XT:860M

The TWINSCAN XT:860M is designed using state-of-the-art optics for volume 300 mm wafer production at and below 110 nm resolution.

TWINSCAN XT:400L

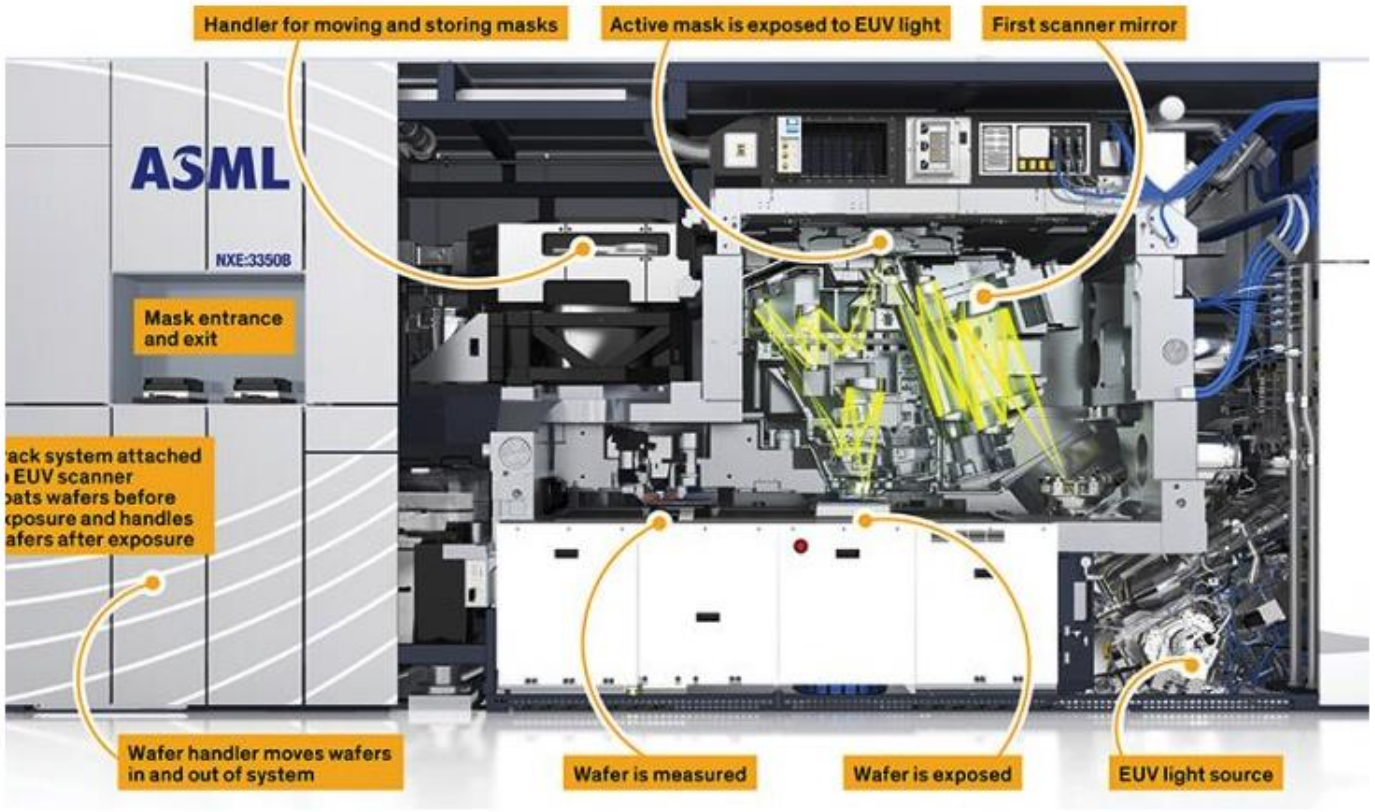
The TWINSCAN XT:400L is ASML's latest-generation i-line lithography system, using a mercury vapor lamp to print features down to 220 nm.

As an example, each TWINSCAN system includes a process chamber as shown below:



See ASML Twinscan Technical Backgrounder, *available at* https://www.chiphistory.org/landmarks/lm_asml_twinscan_step_and_scan_aligner_1990/ip_asml_twinscan_step_and_scan_aligner_1990.htm (annotated).

See also EUV Lithography tools shipping in 2018, available at https://www.nextbigfuture.com/2017/04/euv-lithography-tools-shipping-in-2018.html:



TSMC uses, for example, ASML's extreme ultraviolet (EUV) lithography systems on 5nm and 7nm products. *See e.g.*, TSMC 5nm Technology, *available at* https://www.tsmc.com/english/dedicatedFoundry/technology/5nm.htm ("TSMC's 5nm Fin Field-Effect Transistor (FinFET) process technology is optimized for both mobile and high performance computing applications. It is scheduled to start risk production in the second half of 2019. TSMC's 5nm technology is the second available EUV process technology. It showed promising imaging capability with expected good wafer yield."); *see also TSMC Celebrates 25th Anniversary of the North American Technology Symposium*, *available at* https://www.tsmc.com/tsmcdotcom/PRListingNewsAction.do?action=detail&language=E&newsid=THGOWQTHTH ("The World's first commercially available 7nm EUV in volume production in 2019").

As another example, the TWINSCAN system performs the method of providing a process chamber:

See ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30 2019).

The process chamber can be used for wafer exposure during lithography:

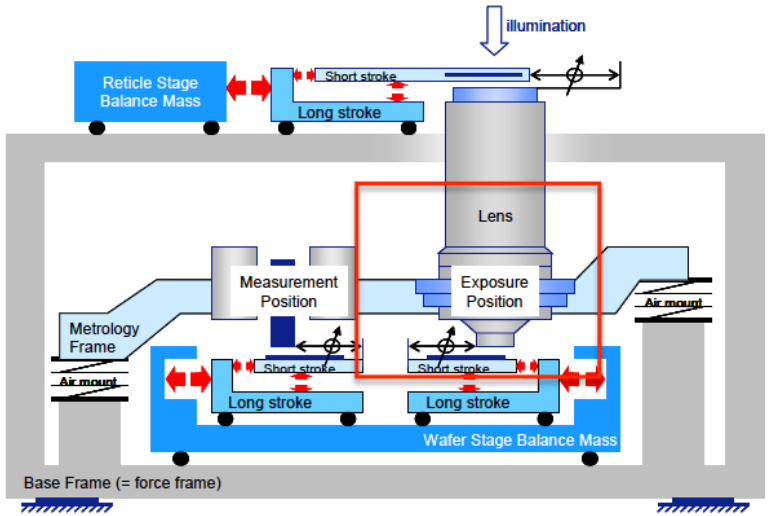


Figure 5. TWINSCAN™ dynamic architecture

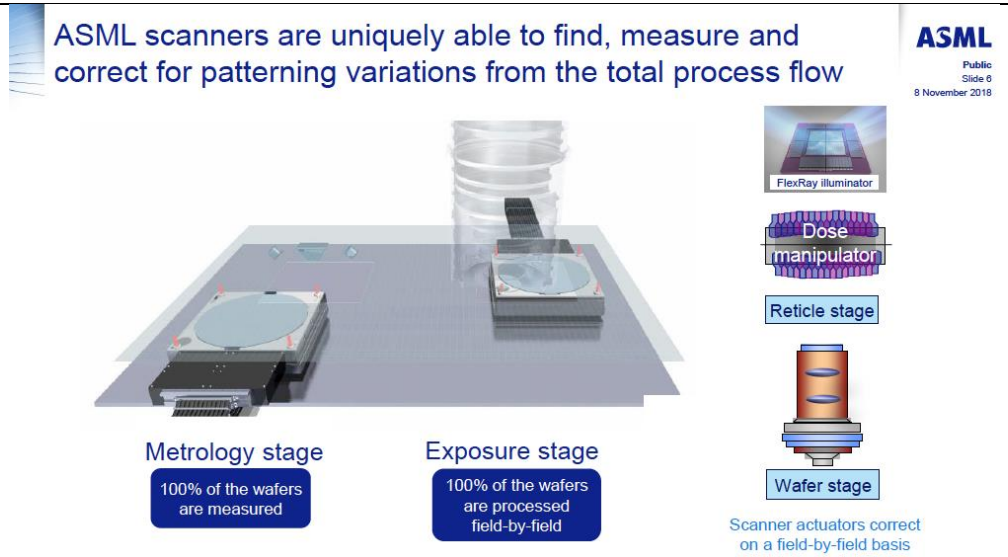
See Perspective on Stage Dynamics and Control at 3.

The process chamber includes an adjustable wafer stage having a surface that is adjustable and located in a first plane:

"In Figure 4, the table holding the wafer is called the mirror block because of the mirroring side surfaces, which allow interferometric position measurement (IFM)."

See Position Control at 31.

For example, the adjustable wafer stage or mirror block (whose surface is located in a first plane) of the TWINSCAN system is shown below:

	 *See* Applications Products and Business Opportunity at 6.
adjusting said surface of said wafer stage by lowering said surface of said wafer stage to a position wherein said surface of said wafer stage is positioned in a second plane that is offset from and approximately parallel to said first plane;	The ’651 Infringing Instrumentalities adjust the surface of the wafer stage by lowering the surface of the wafer stage to a position. The mirror block or wafer stage of the TWINSCAN system has a surface that can be lowered using vertical actuators (e.g., in the “z direction”): “Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively.” *See* Position Control at 41; *see also id.* at 38 (“For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metroframe world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor.”). As an example, the TWINSCAN system includes a linear motor to drive the wafer stage in the x direction while simultaneously acting as a guiding beam for a roller bearing. The x motor itself is moved in the y direction as well

	as in the rotational direction θ around the z axis: "One linear motor drives the stage in the x direction, while simultaneously acting as a guiding beam for a roller bearing. The x motor itself can be moved in the y direction as well as in a rotational direction u around the z axis, by means of two linear y motors. These motors also act as a guiding beam for the bearings of the x-motor stators." *See* Position Control at 31. Also, the wafer stage's stage coordinates for lowering are defined by X, Y, and Z coordinates: "The next step is then the conversion of forces in the stage coordinate system into forces $f^{T}m$ = (Fx1 Fy1 Fy2 Fz1 Fz2 Fz3) for the individual motors. This step, which is called gain balancing, is completely determined by the geometric actuator layout." *See* Position Control at 41. As an example, the vertical directions (e.g., lowering) of the wafer stage can be achieved using Lorentz actuators: "To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result" *See* Position Control at 40. A diagram showing the vertical connection that facilitates the vertical movement (including lowering) of the wafer stage is shown below:

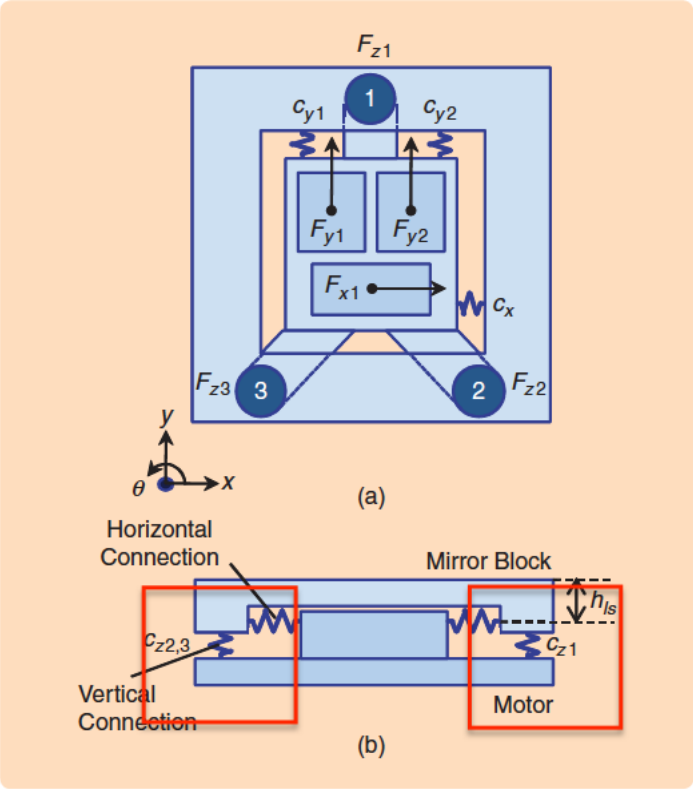


FIGURE 26 Stage layout with motor connection stiffness. The motor

See Position Control at 41 (annotated).

In one example, the wafer stage rotates around the center of the lens above it in the vertical directions:

"The stage now rotates around the lens center instead of its center of mass. Especially in the vertical directions, the applicable rotations may show a high acceleration, depending on the vertical topology of the wafer surface."

See Position Control at 42.

As yet another example, the wafer is lowered from the projection lens such that it is offset from and approximately parallel to its previous position in the first plane.

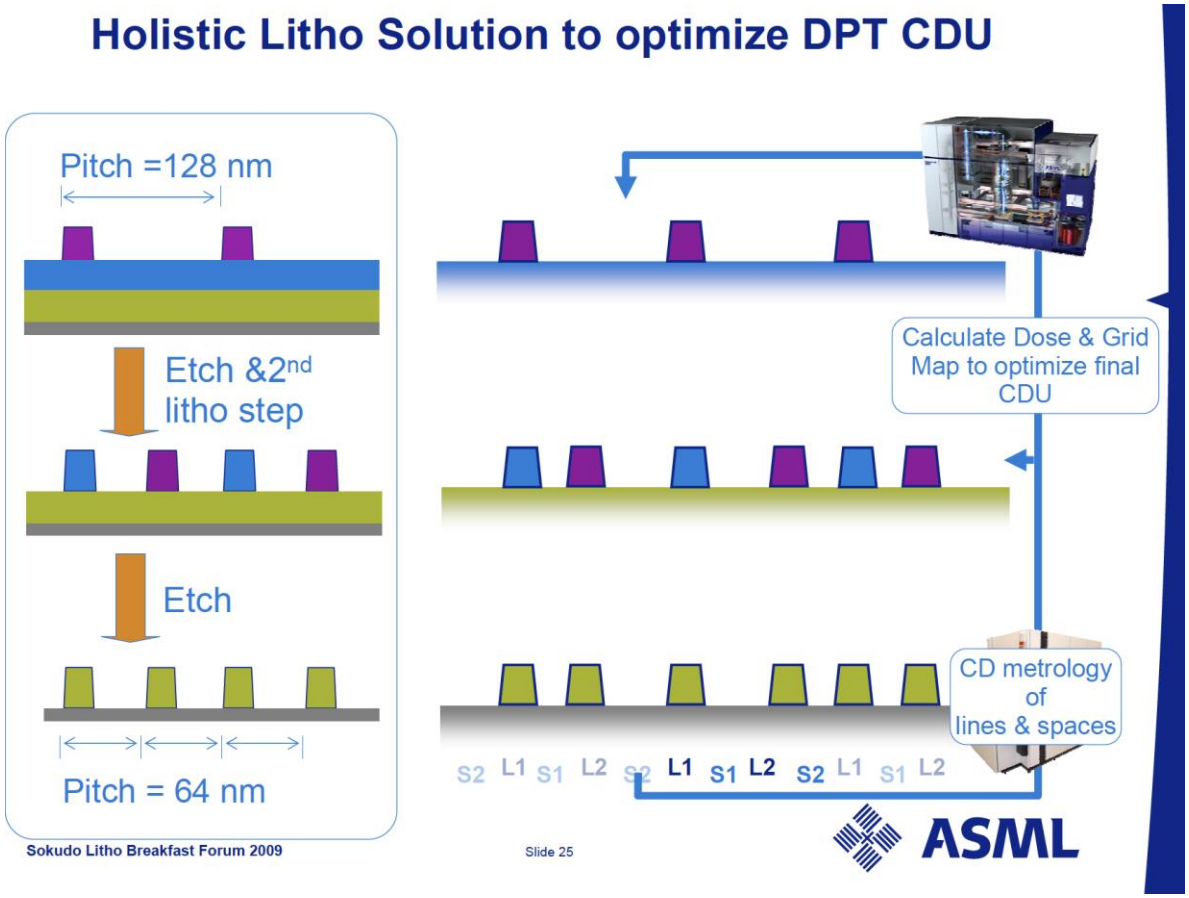
positioning a wafer on	The '651 Infringing Instrumentalities position a wafer on the wafer stage.

said wafer stage; and	For example, the TWINSCAN system positions the wafer on the wafer stage: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35. The wafer is also positioned onto the wafer stage so that exposure can start: "At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40.
performing a process operation on said wafer positioned on said wafer stage.	The '651 Infringing Instrumentalities perform a process operation on the wafer position on the wafer stage. For example, the TWINSCAN system performs stepper imaging or double patterning as part of the step-and-scan in exposing a wafer: "After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging." *See* Position Control at 35. Once the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself, the stage positioned under the projection lens is aligned to the reticle by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start: "Stage position measurement is now performed in all degrees of freedom by interferometers, with reference beams directed at the projection lens. This method provides a direct relative measurement of the position with respect to the lens. At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with

	respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start." *See* Position Control at 40. As another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage, as shown below: "A solution was found by equipping the system with two wafer stages [7]. While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. The increased stage acceleration and speed further improves throughput." *See* Position Control at 39-40; *see also id*. at 37: "Figure 16 shows a more detailed timing diagram of the stage movement during a scan. Figure 16(b) shows an acceleration setpoint profile, which in this example is a thirdorder profile instead of the previously used second-order profile. Figure 16(a) shows the velocity setpoint profile. At t5t0, the acceleration phase ends, and a constant velocity is reached. After a certain settling time, which allows the remaining controller error to be reduced to an acceptable value, the first point in the die to be exposed enters the illumination slit at t5t1. At t5t2, this first point on the die leaves the slit again. The stage-positioning errors in the interval 3t1, t2 4 determine the effect on overlay and imaging. Hence, the calculated MA and MSD values over this first interval correspond to the effect of positioning errors on the first point in the die. At t5t3, the last point of the die enters the slit, and, finally, at t5t4 the die leaves the slit again, making the interval 3t3, t4 4 the last window over which MA and MSD values need to be calculated. Hence, the total scan length of the stage equals the length of the die, plus the height of the slit, plus the length needed for settling of the stage. After t5t4, the stage decelerates again to standstill or follows another trajectory that brings the stage to the start of the next die." As a further example, "the ASML® TWINSCAN® NXE:3350B production-ready EVU system produces 125 computer wafers per hour using 13.5 nm wavelength light." *See* V. Marra, "ASML Advances Computing

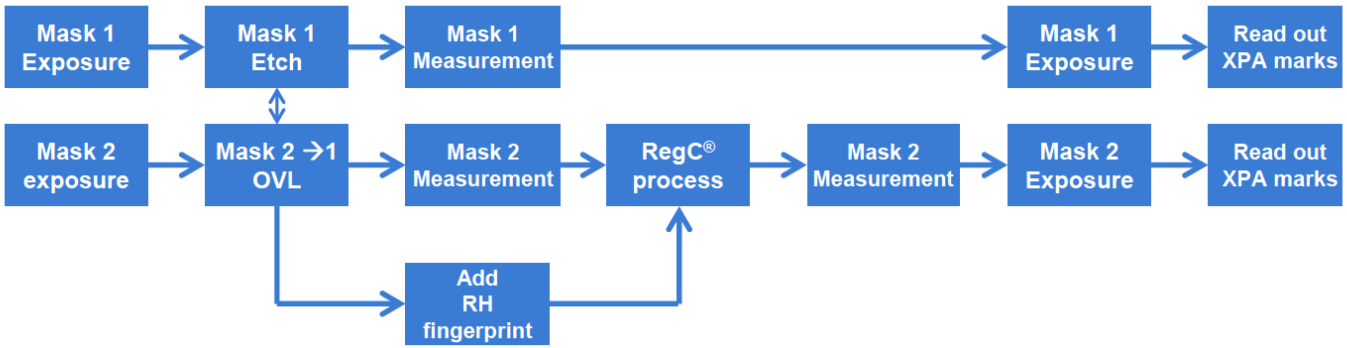
Breakthroughs with Multiphysics Modeling" at 4.

As yet another example, the TWINSCAN system performs a process operation on the wafer position on the wafer stage:



See Holistic View of Lithography 25.

As a further example, the '651 Infringing Instrumentalities, including the TWINSCAN system, perform "Mask 1 Etch":



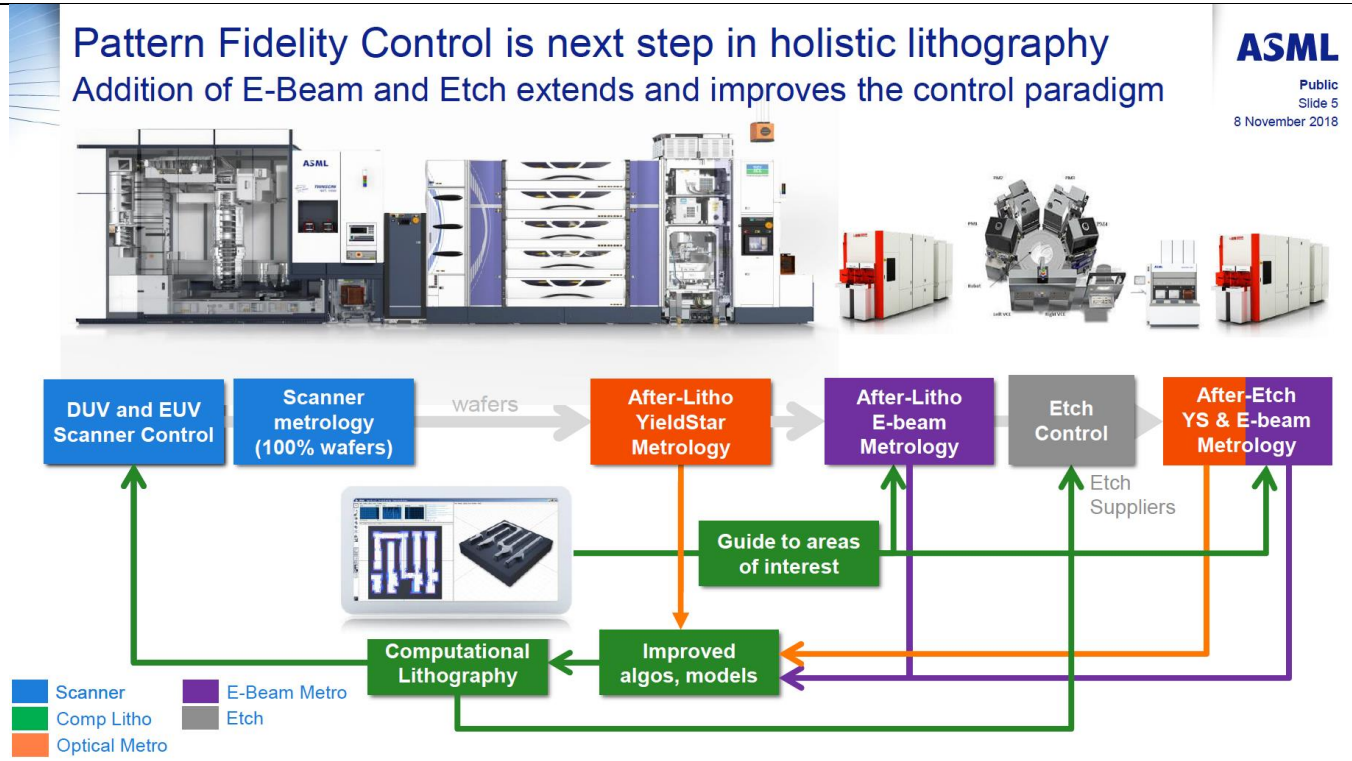
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM Corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes:

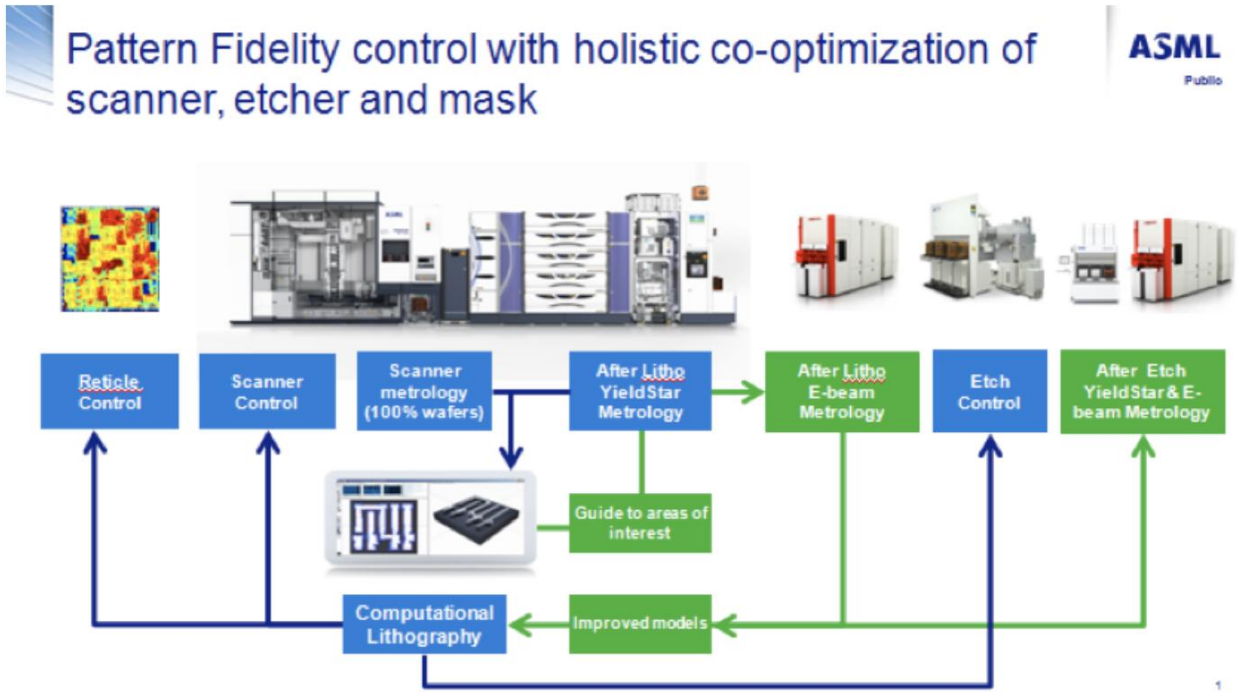
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

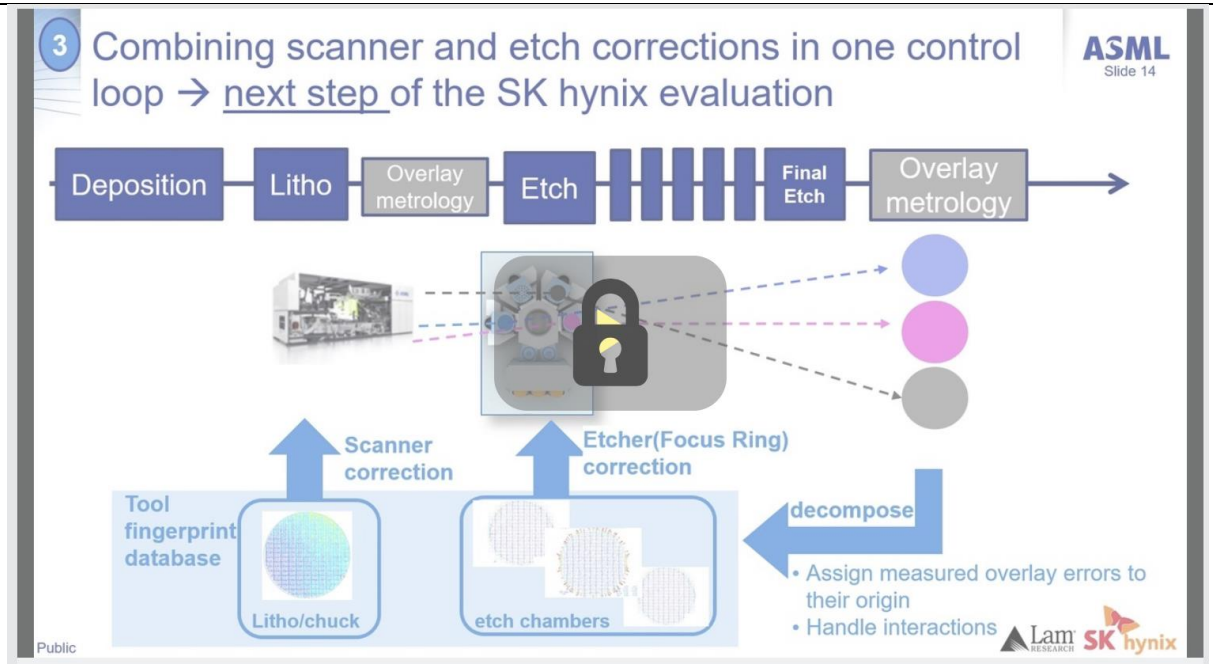
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:



(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

See Process Complexity at 2; *see also* Scanner and Etch Co-optimized Corrections (showing "combining scanner and etch corrections in one control"):



78. The method of claim 77, wherein positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage after said wafer stage has been adjusted.	The ’651 Infringing Instrumentalities position a wafer on the wafer stage after said wafer stage has been adjusted. For example, the TWINSCAN system positions the wafer on the exposure table of the dual-wafer stage after the exposure of a previous wafer is done and the exposure table is adjusted to receive a new wafer for the next cycle of exposure. *See, e.g.*, P. Drabik, “Performance prediction for Stage Positioning Measurement (SPM),” Master’s Thesis, Eindhoven University of Technology, Department of Mathematics and Computer Science, *available at* https://pure.tue.nl/ws/files/72326295/Master_Thesis_Pawel_Drabik_Public.pdf (“Stage Positioning Management”) at 1-2: “These systems are designed as wafer scanners which Performance prediction for Stage Positioning Measurement (SPM) 1 CHAPTER 1. INTRODUCTION perform the exposure process in step and scan fashion as presented in Figure 1.1. The reticle with circuit pattern is placed on a reticle stage (RS), whereas the silicon wafer is placed on a wafer stage (WS). During the scan movement the light is switched on with a desired dose and the exposure process starts. The stages move according to each other performing synchronized zig-zag movements. Next during the step movement the light is switched o

	, the reticle goes back to its initial position and the silicon wafer is prepared for exposure of a next die. The process repeats itself until all of the dies have been processed. Next, the reticle mask is replaced with a new one and the process can start all over again, exposing a new layer on top of the previous one. The exposure of consecutive layers needs to be done with nanometer precision in order to deliver highest quality circuits."
79. The method of claim 77, wherein positioning a wafer on said wafer stage comprises positioning a wafer on said wafer stage before said wafer stage is adjusted.	The '651 Infringing Instrumentalities position a wafer on a wafer stage before the wafer stage is adjusted. For example, the TWINSCAN system positions the wafer on the measurement table of the dual-wafer stage before the stage position of the measurement table is adjusted: "While the first stage exposes the wafer, the second stage unloads the previous wafer from the tool, loads a new wafer on the stage, aligns the horizontal placement of the wafer on the stage, and measures the wafer height map used to focus the wafer during exposure. When both stages are finished with their tasks, the stages are swapped and a new cycle begins. In this way, the number of wafers that is processed is enlarged by removing overhead time from the expose cycle. T." *See* Position Control at 35. *See also* Stage Positioning Management at 3:

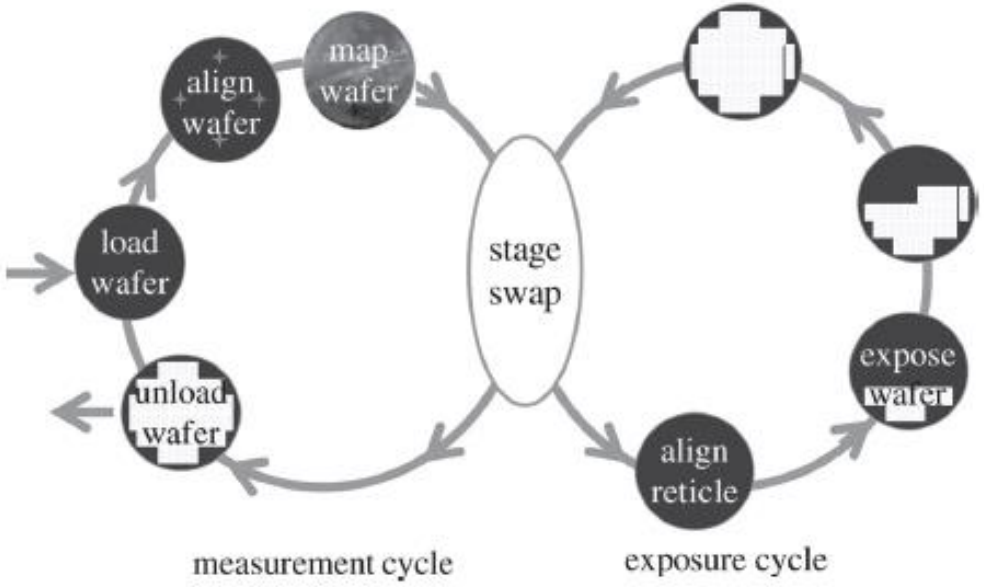
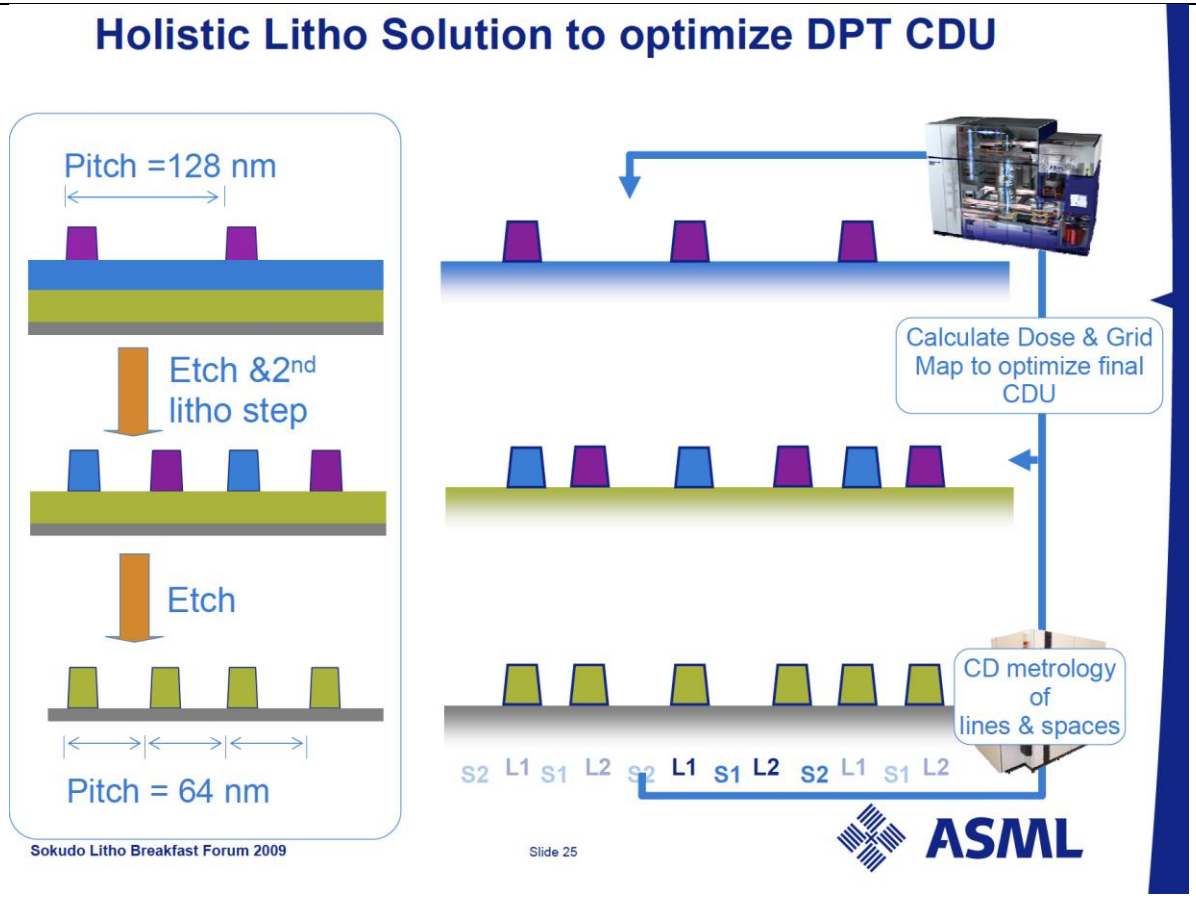


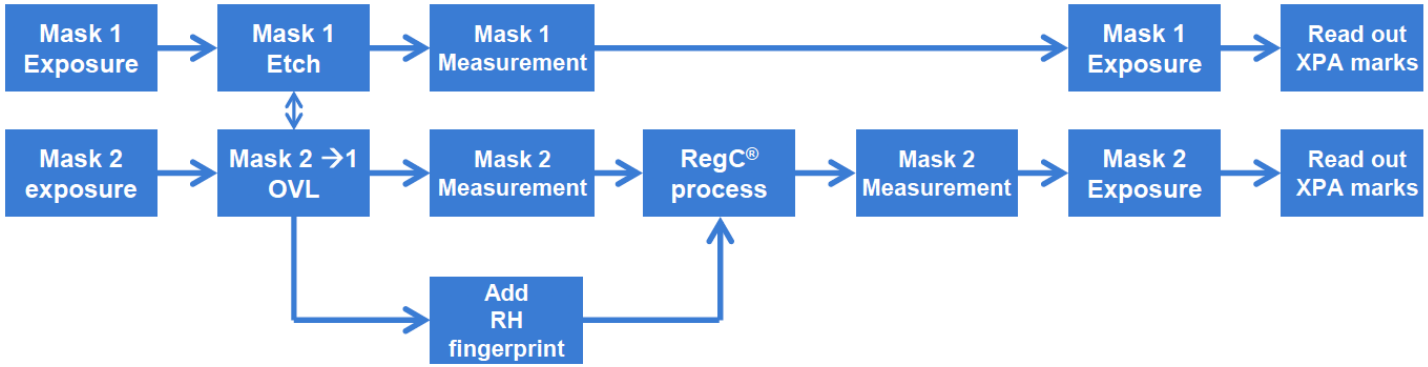
Figure 1.3: The process steps in TWINSCAN machine [18]

80. The method of claim 77, wherein performing a process operation on said wafer comprises performing at least one of a deposition process and an etching process on said wafer in said process chamber.	The '651 Infringing Instrumentalities perform a process operation on the wafer comprises performing at least one of a deposition process and an etching process on the wafer in the process chamber. For example, the TWINSCAN system perform a process operation on the wafer comprises performing at least an etching process on the wafer in the process chamber:



See Holistic View of Lithography at 25.

As a further example, the ’651 Infringing Instrumentalities, including the TWINSCAN system, perform “Mask 1 Etch,” as shown below:



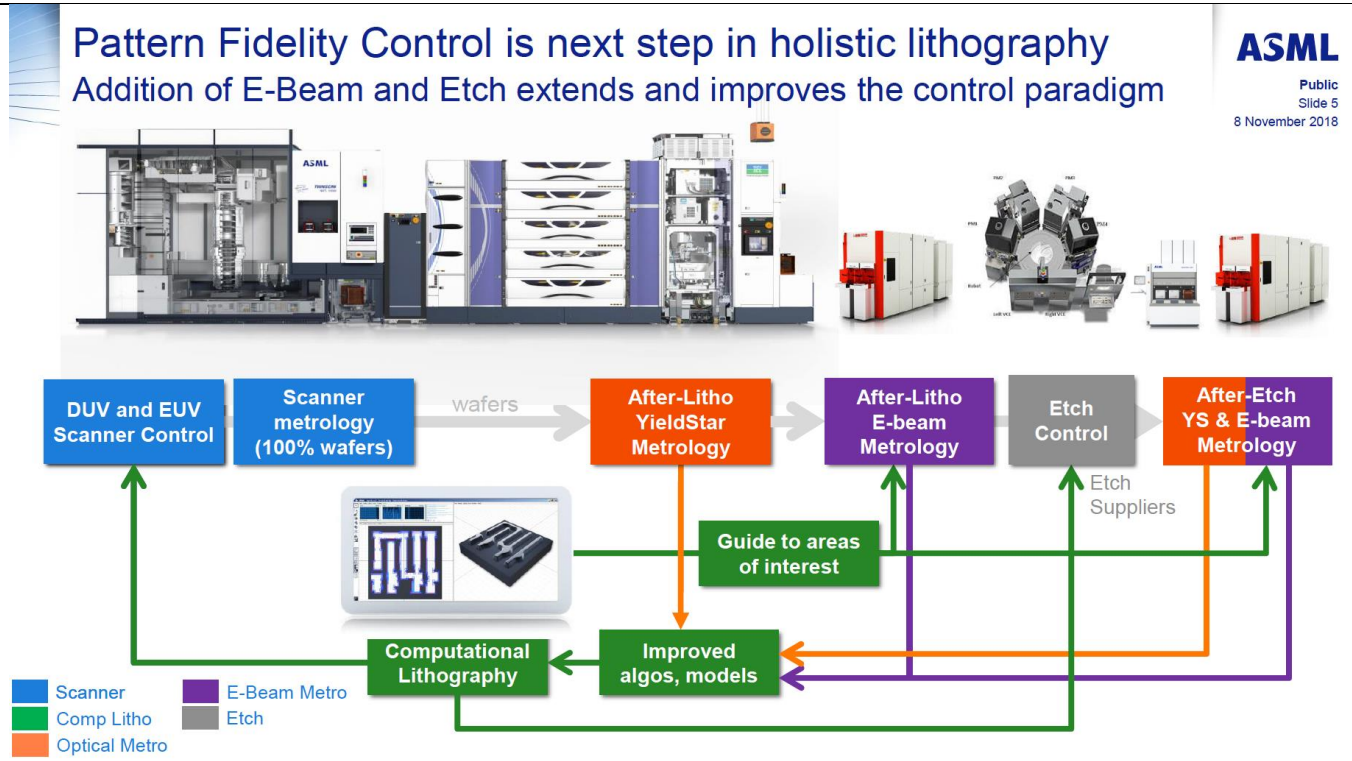
"Figure 10. Work flow overview for test 2: imposing a pre-defined counter reticle heating fingerprint into the reticle to extend the TWINSCANTM K18 actuator range and reduce the intra-field overlay. The ASML TWINSCANTM was used for XPA read outs and the exposures. The RegC® tool was used to induce the pre-defined fingerprint into the reticle and correct the intra-field fingerprint."

See Co-optimization of RegC® and TWINSCANTM Corrections at Fig. 10.

As a further example, the'651 Infringing Instrumentalities perform etch and deposition processes, as shown below:

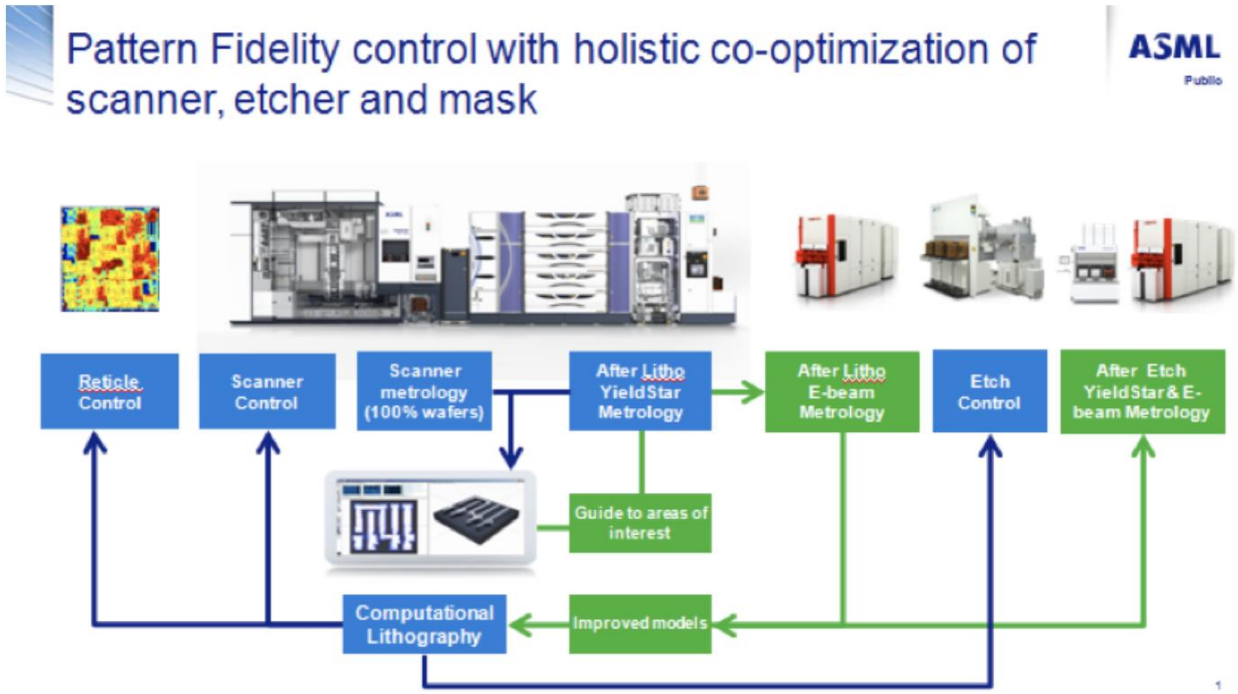
See Machine Learning in Computational Lithography at 15.

As a further example, the ’651 Infringing Instrumentalities perform etching, as shown below:



See J. Koonmen, "Applications Products and Business Opportunity," at 5.

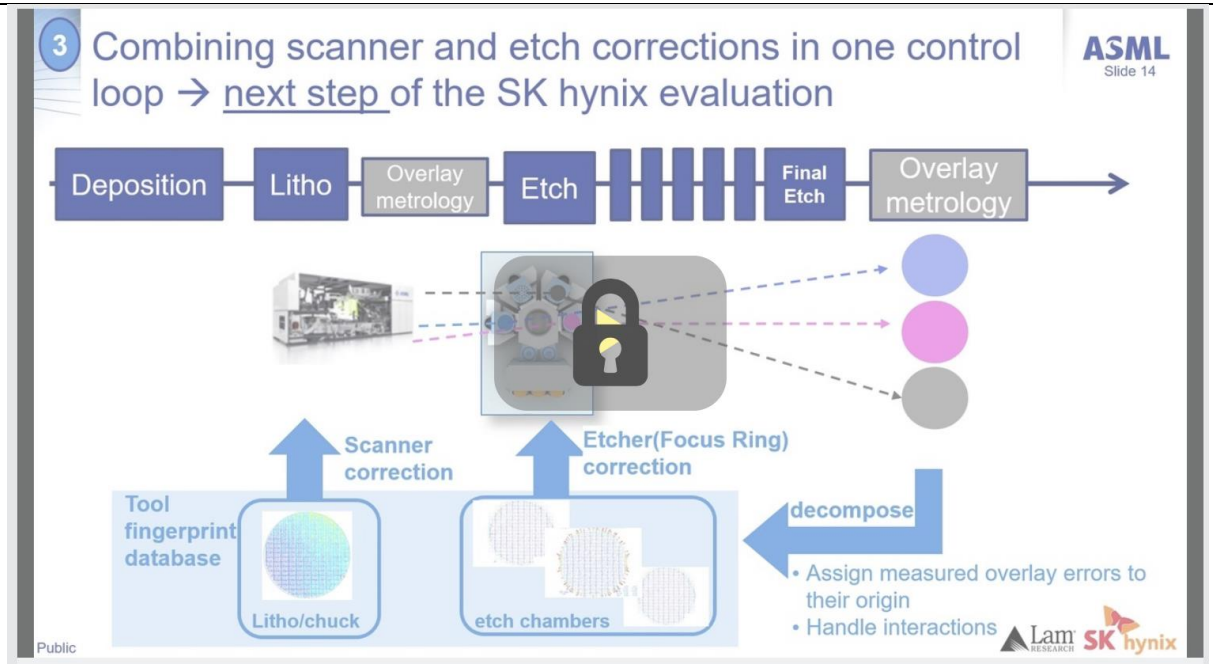
As a further example, the '651 Infringing Instrumentalities "co-optimize[] its scanner process with etch and reticle process steps," as shown below:



(https://electroiq.com/wp-content/uploads/2018/07/process-complexity.png)

ASML co-optimizes its scanner process with etch and reticle process steps. Source: ASML

See Process Complexity at 2; *see also* Scanner and Etch Co-optimized Corrections (showing "combining scanner and etch corrections in one control"):



As a further example, the'651 Infringing Instrumentalities also include a chamber for deposition of pin-on-glass, anti-reflective coating and photoresist, as shown below:

"Patterning was achieved by depositing 100nm SOC, 30nm spin-on-glass (SOG), 29nm Anti-Reflective Coating (ARC), and 105nm photoresist (PR) in an ASML Twinscan NXT:1950i 193nm immersion scanner, followed by lithographic patterning of line/space patterns."

See Atomic Layer Deposition at 8.

81. The method of claim 77, wherein adjusting said surface of said wafer stage comprises adjusting said surface of said wafer stage by actuating at least one of a plurality of	The '651 Infringing Instrumentalities adjust the surface of the wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage. For example, the TWINSCAN system actuates six Lorentz actuators that are mounted between the air foot and the wafer stage: "Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and Ψ, respectively."

pneumatic cylinders that are operatively coupled to said wafer stage.	*See* Position Control at 41. Generally, the wafer stage is equipped with DOF Lorentz actuators (e.g., three DOF actuators for the horizontal directions and three DOF actuators for the vertical directions): "The table also had vertical movement directions for the purpose of focusing the wafer in the image plane of the lens, requiring a measurement of the distance of the wafer to the lens by means of a level sensor system. The horizontal stage position was measured by an interferometer system. The stage was guided by means of mechanical bearings 'rolling' over the motor beams. With regard to controlling the stage, the horizontal controllers (3-DOF) acted independently from the vertical directions (also 3-DOF)." *See* Perspective on Stage Dynamics and Control at 1. As an example, for the x and y direction, the wafer table is adjusted by three Lorentz actuators such that the stage floats over a granite stone by means of an air bearing and the Lorentz actuators are connected to this granite stone:

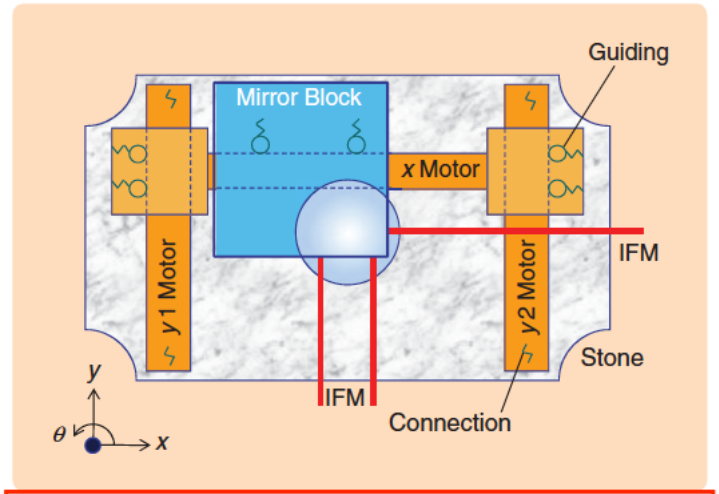


FIGURE 5 Wafer stage top view. The wafer table is driven by three actuators, two of which drive the stage in the *y* direction and the remaining one in the *x* direction. The linear actuators also function as a guide for the horizontal motion, cooperating with ball bearings in the mover. The stage floats over a granite stone by means of an air bearing, and the linear actuators are connected to this stone as well. Interferometers measure the stage position, making use of mirroring side surfaces of the stage.

See Position Control at 31 (annotated).

In total, the TWINSCAN includes 6-DOF Lorentz actuators and 6-DOF stage control, in addition to offline leveling:

"In TWINSCAN™, a further perfection in the basic design was made by using balance masses, full 6-DOF Lorentz actuators and 6-DOF stage control, in addition to off-line levelling."

See Perspective on Stage Dynamics and Control at 3.